

FIG. 1

PRIOR ART



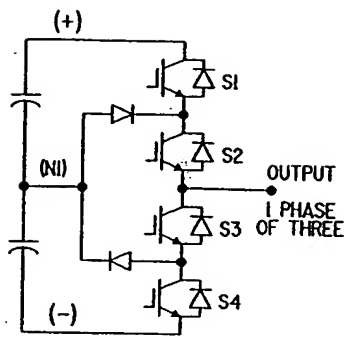


FIG. 3A  
PRIOR ART

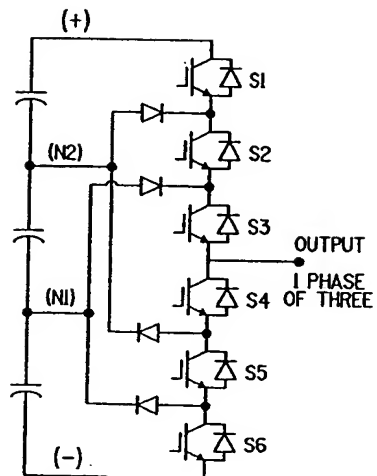


FIG. 3B  
PRIOR ART

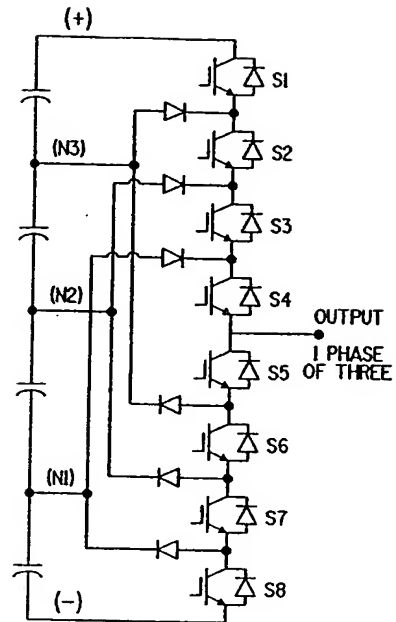


FIG. 3C  
PRIOR ART

SWITCH STATE		OFF	ON
<u>3 LEVEL</u>	1)	S1,S2	S3,S4
	2)	S1,S4	S2,S3
	3)	S3,S4	S1,S2
<u>4 LEVEL</u>	1)	S1,S2,S3	S4,S5,S6
	2)	S1,S2,S6	S3,S4,S5
	3)	S1,S5,S6	S2,S3,S4
	4)	S4,S5,S6	S1,S2,S3
<u>5 LEVEL</u>	1)	S1,S2,S3,S4	S5,S6,S7,S8
	2)	S1,S2,S3,S8	S4,S5,S6,S7
	3)	S1,S2,S7,S8	S3,S4,S5,S6
	4)	S1,S6,S7,S8	S2,S3,S4,S5
	5)	S5,S6,S7,S8	S1,S2,S3,S4

FIG. 4A

FIG. 4B

FIG. 4C

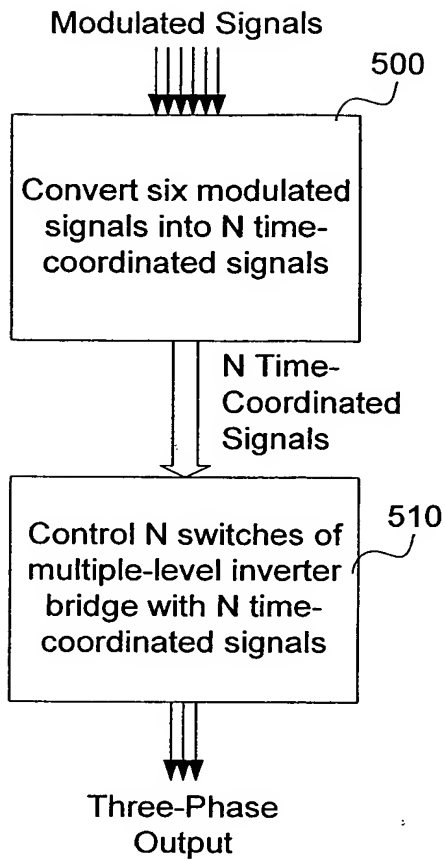


FIG. 5

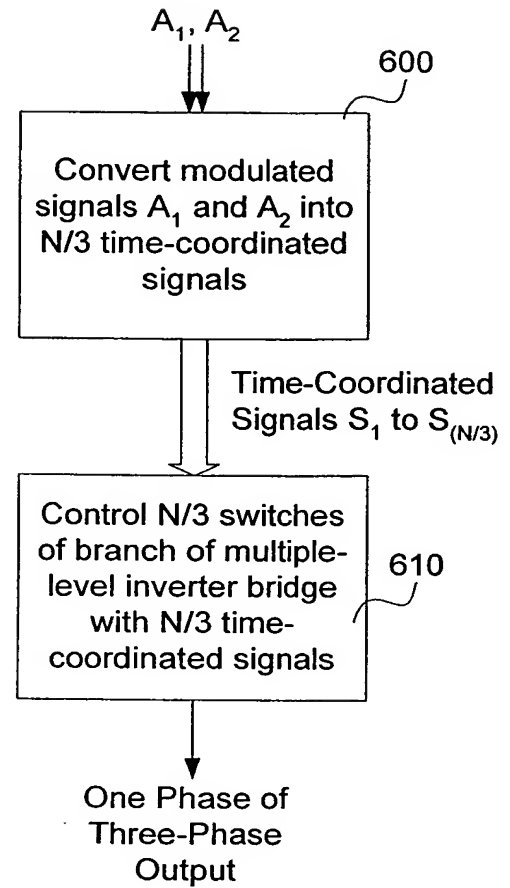
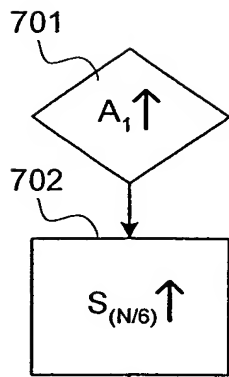
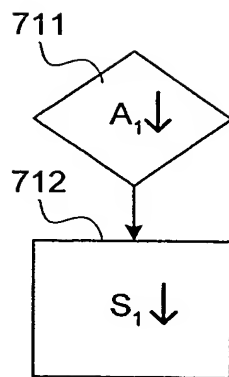


FIG. 6



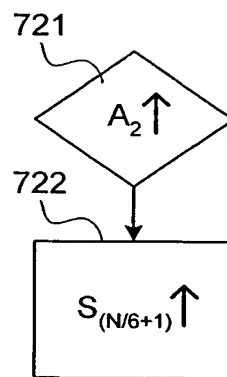
$y = 1 \text{ to } N/6-1$

FIG. 7A



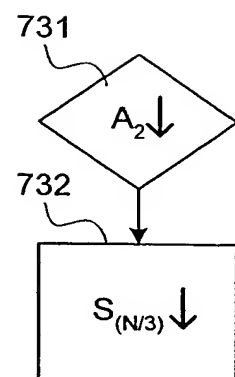
$y = 1 \text{ to } N/6-1$

FIG. 7B



$z = N/6+2 \text{ to } N/3$

FIG. 7C



$z = N/6+2 \text{ to } N/3$

FIG. 7D

FIG. 8A

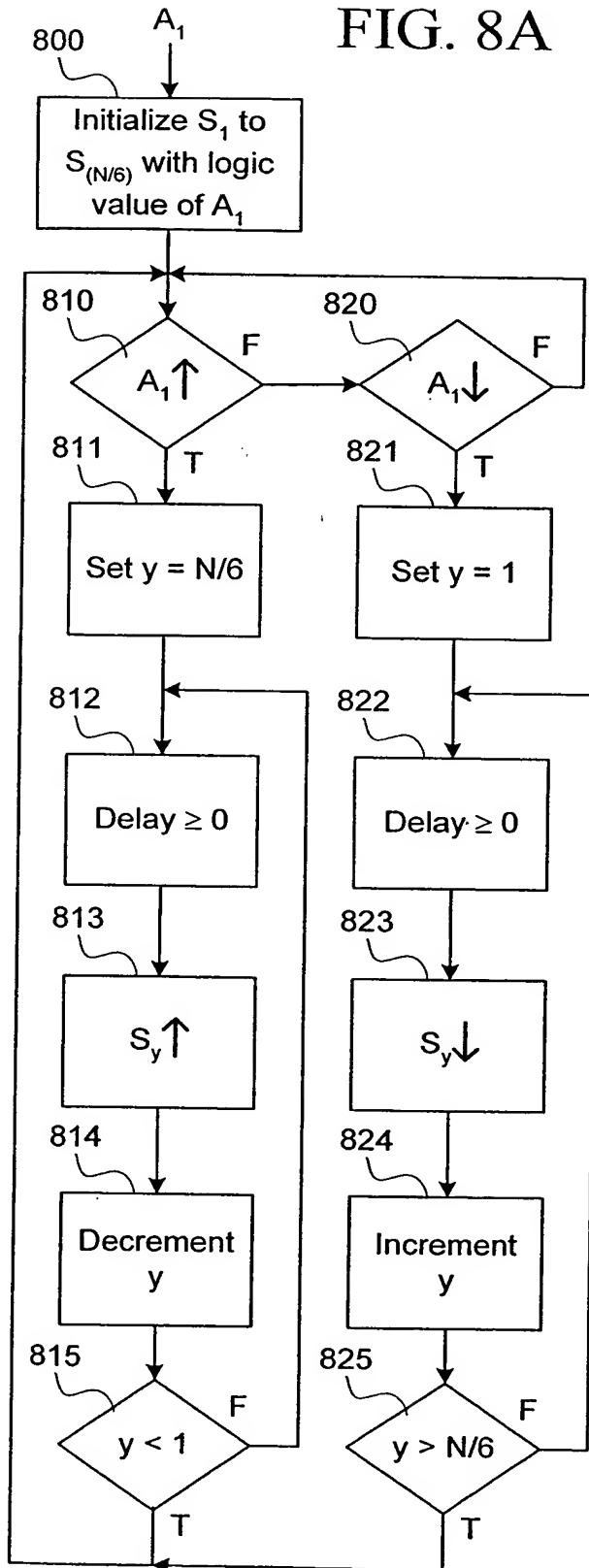


FIG. 8B

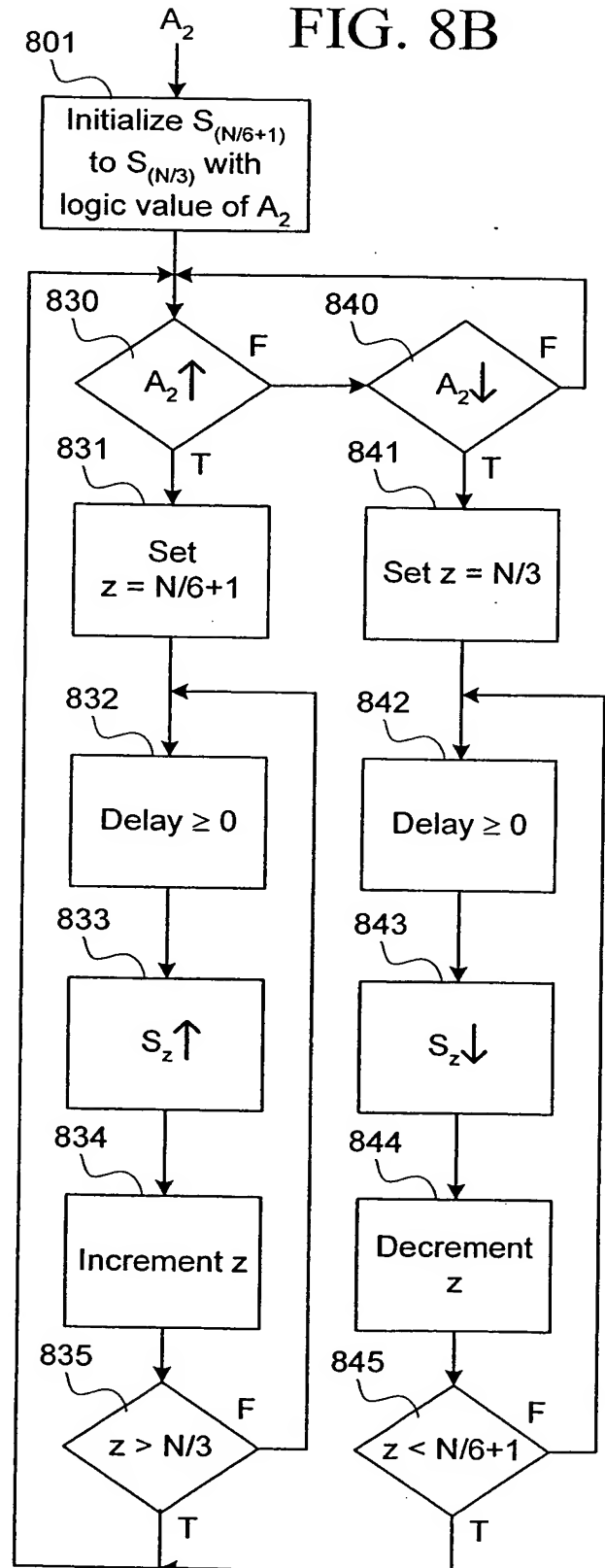


FIG. 9A

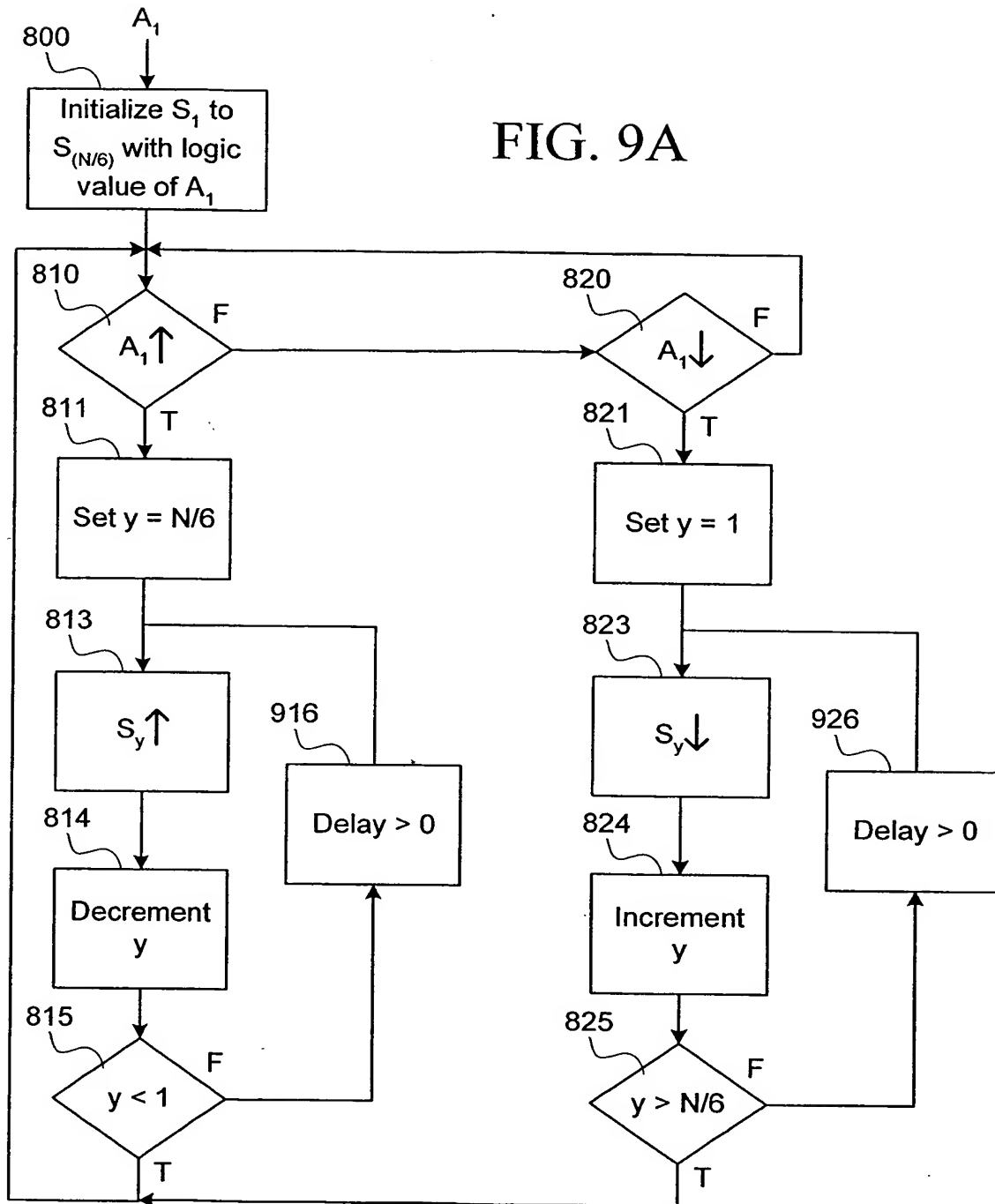
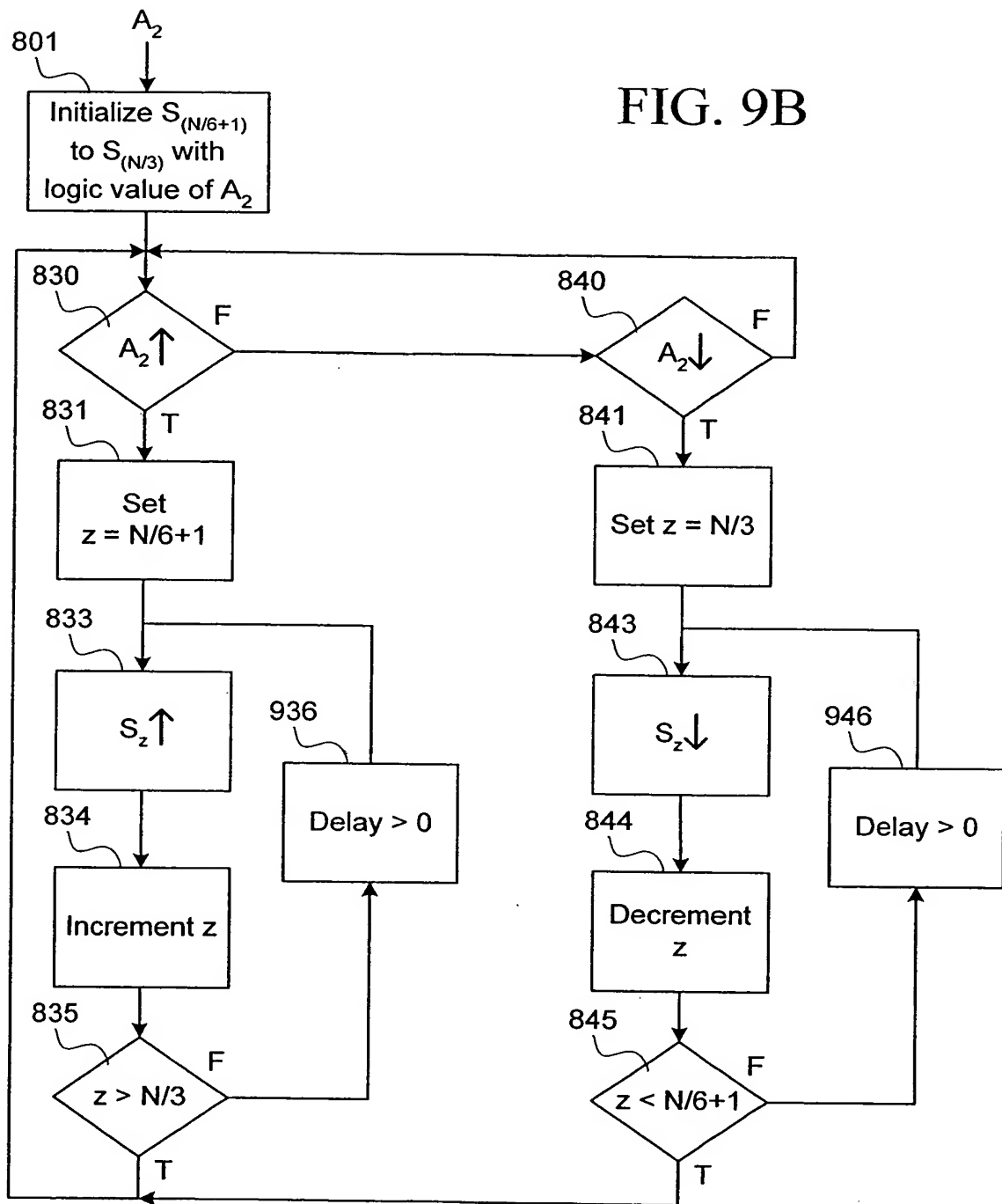


FIG. 9B



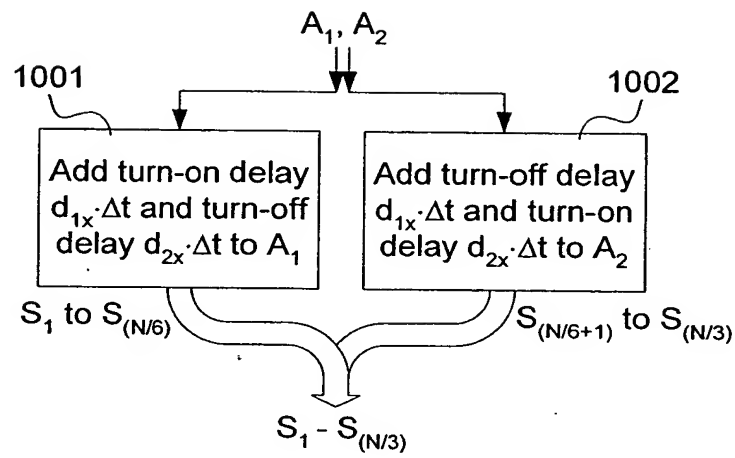


FIG. 10

FIG. 11

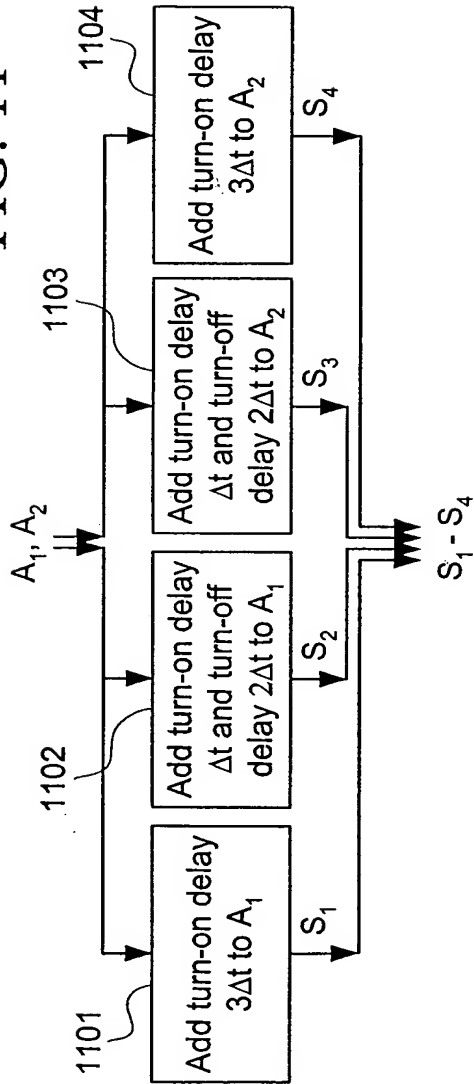


FIG. 12

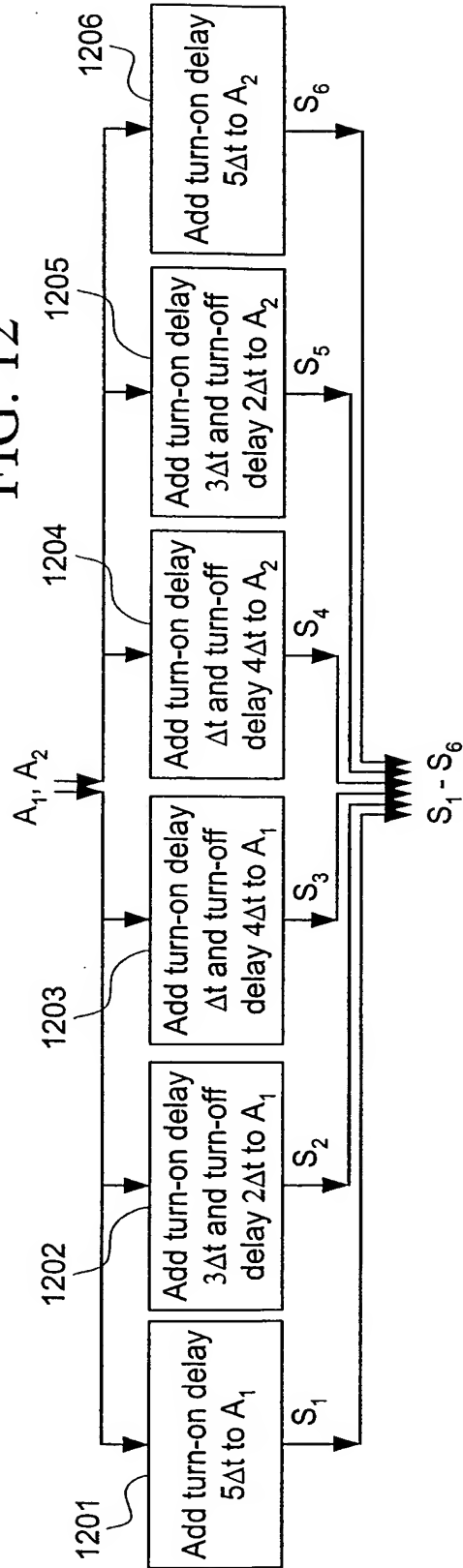
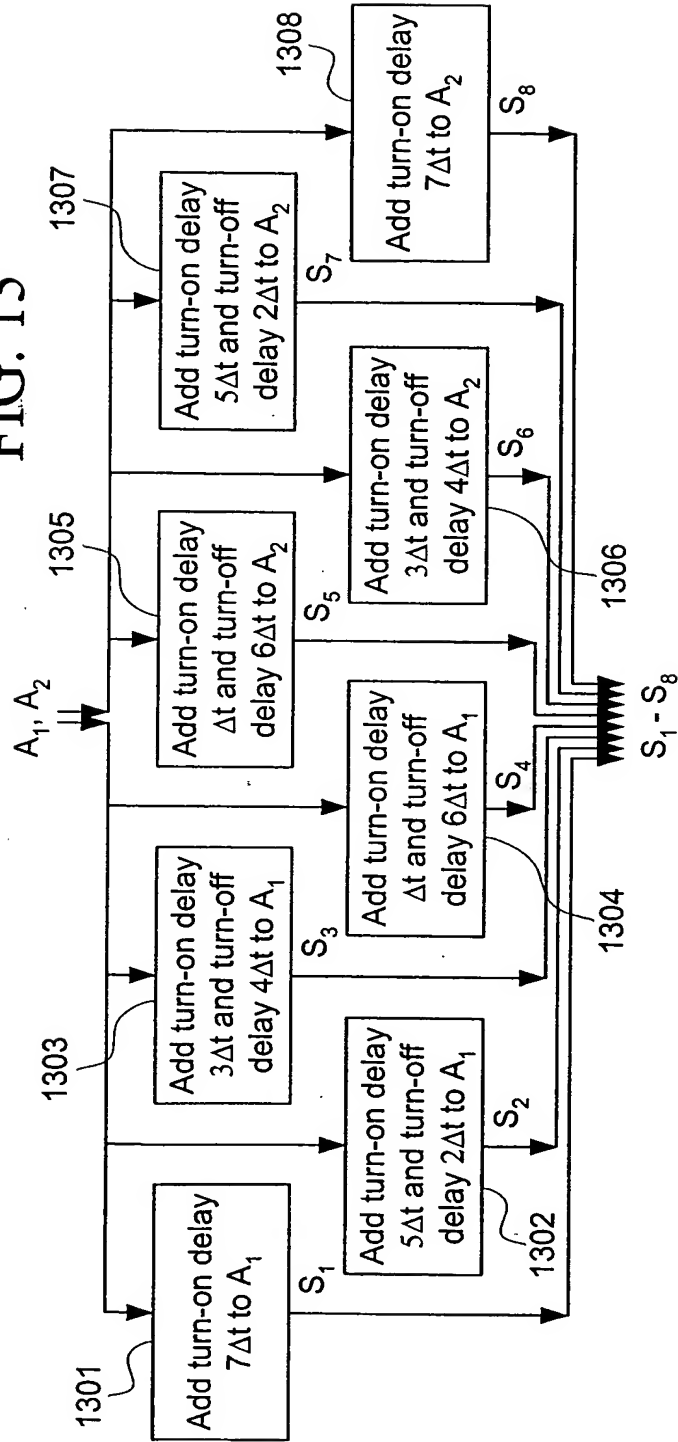


FIG. 13



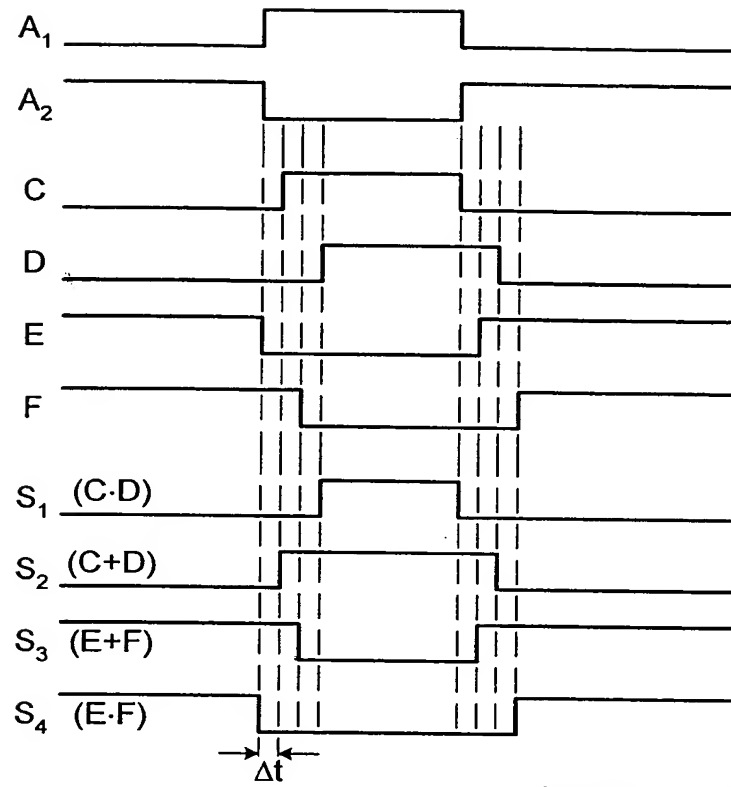


FIG. 14

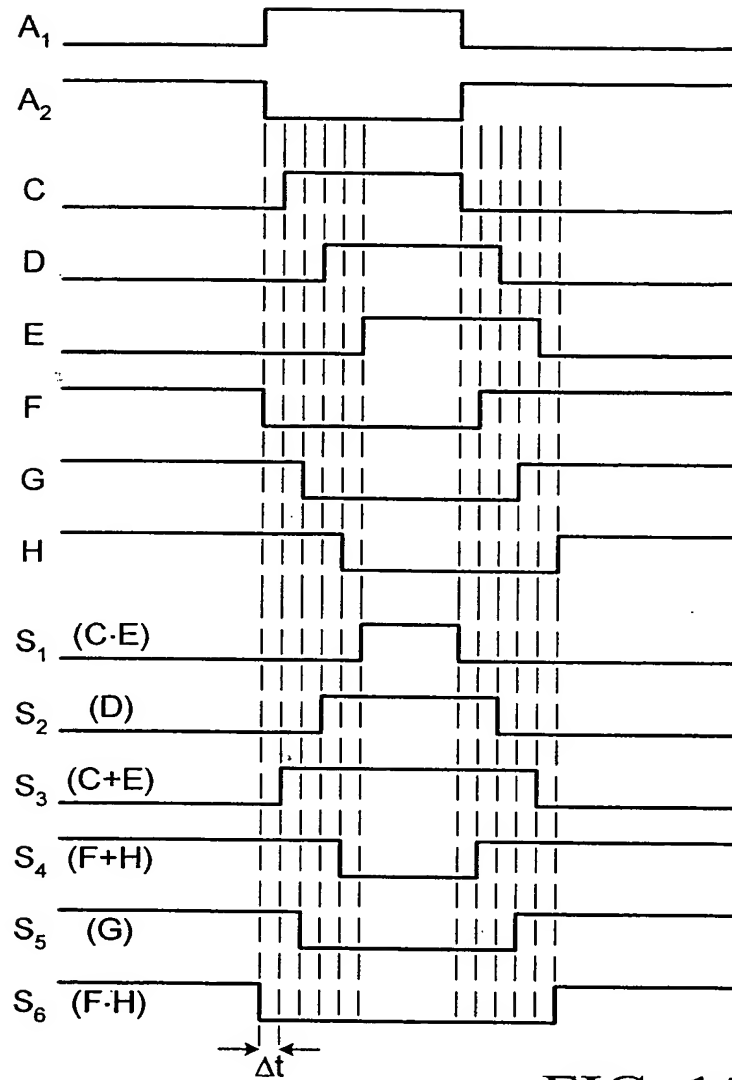


FIG. 15

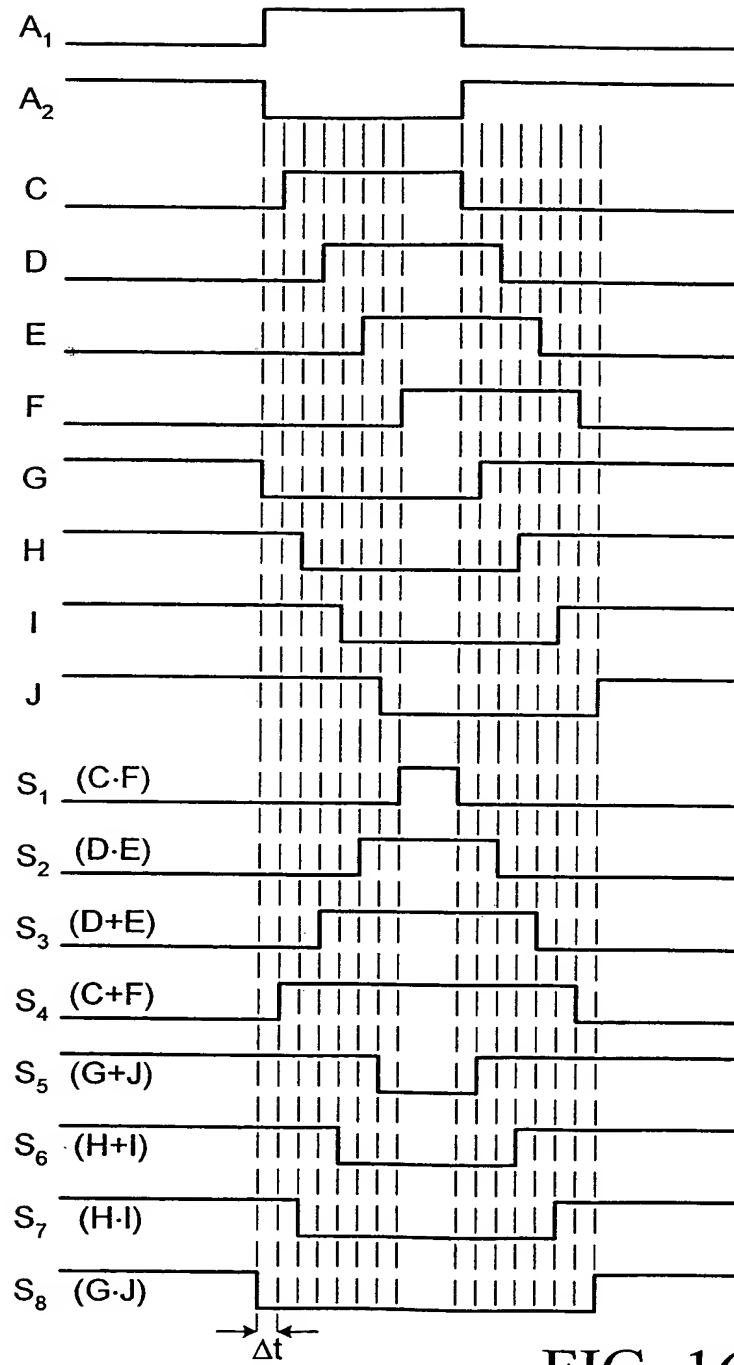


FIG. 16

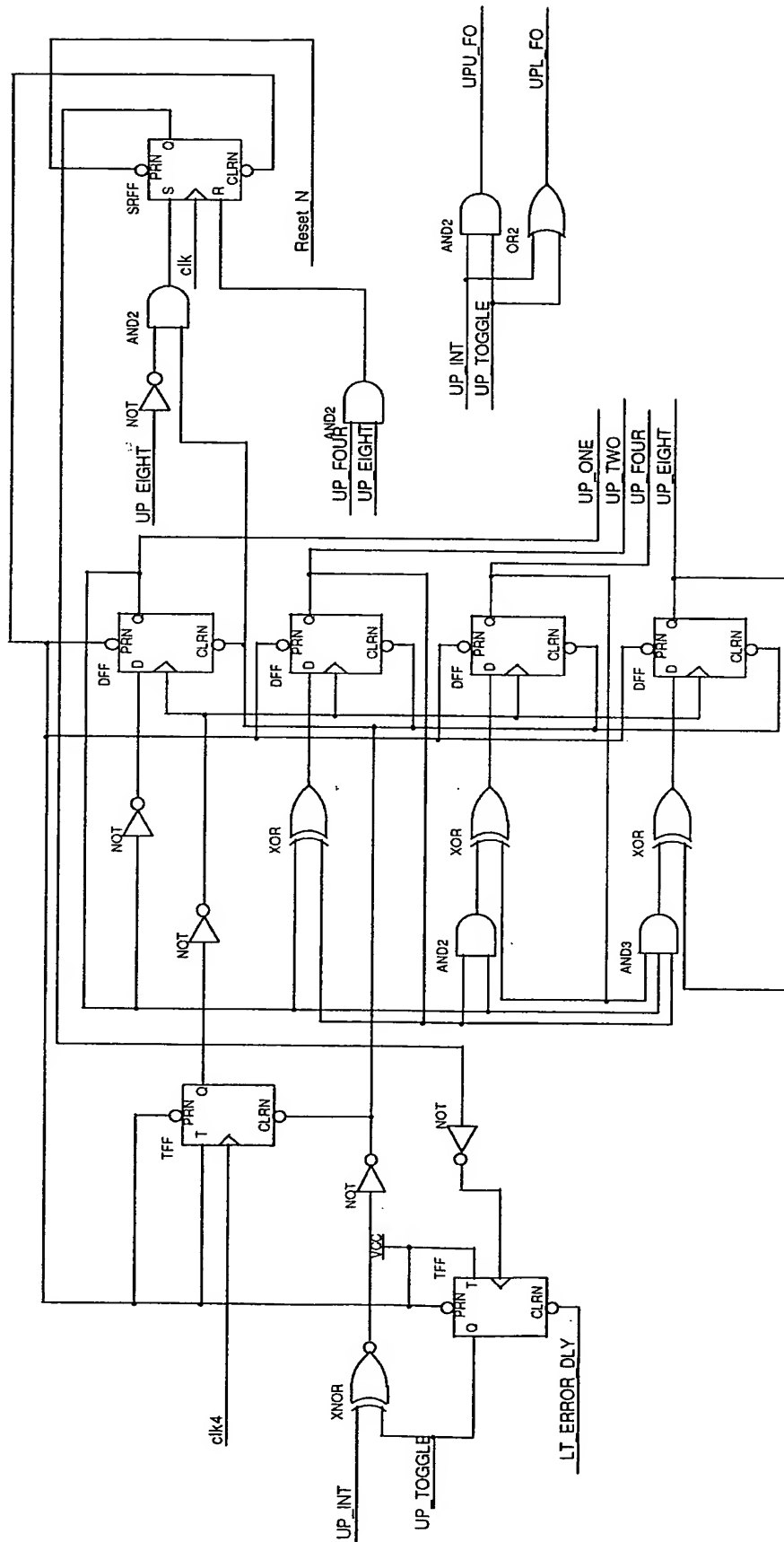


FIG. 17A

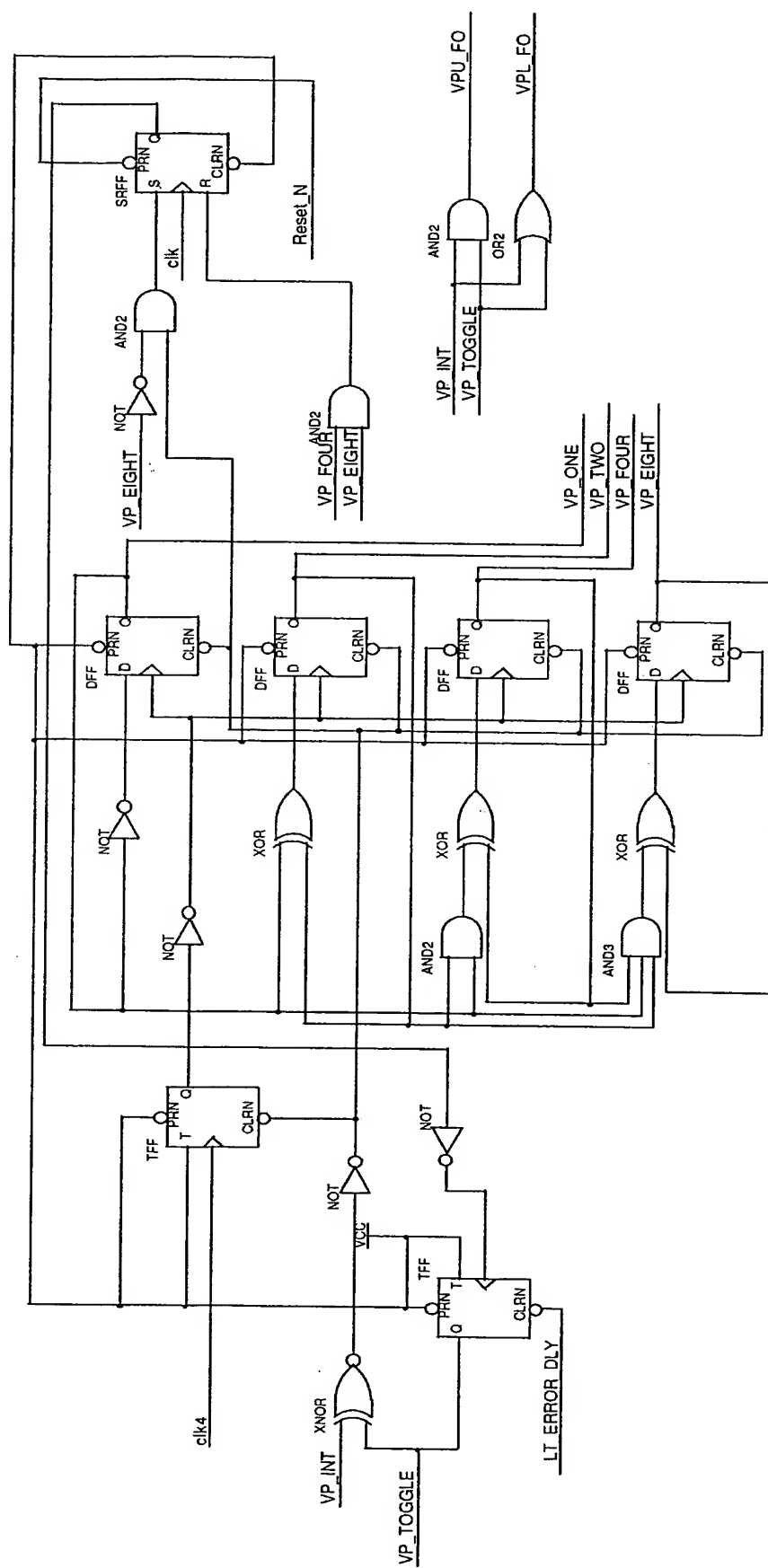


FIG. 17B

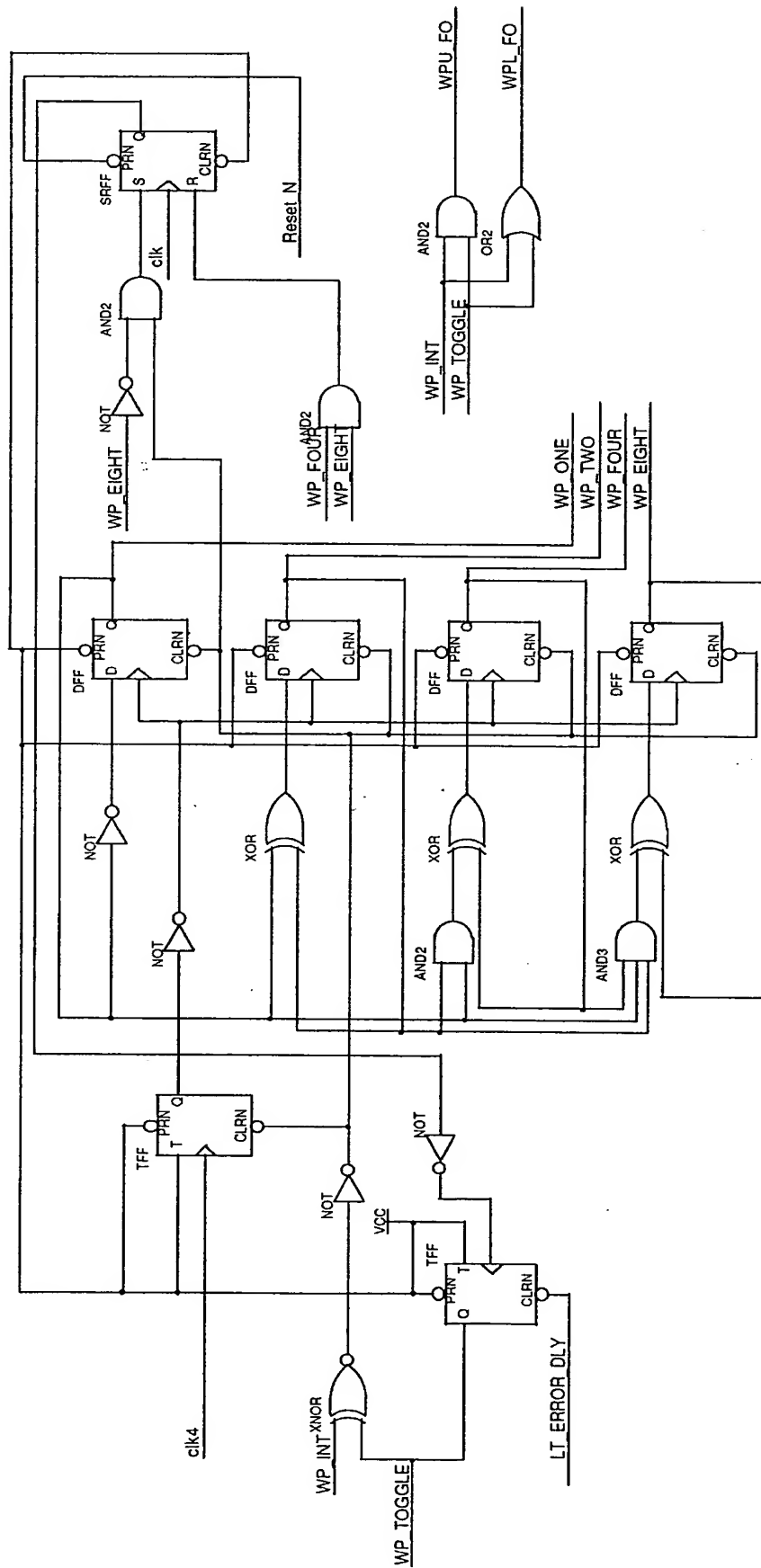


FIG. 17C

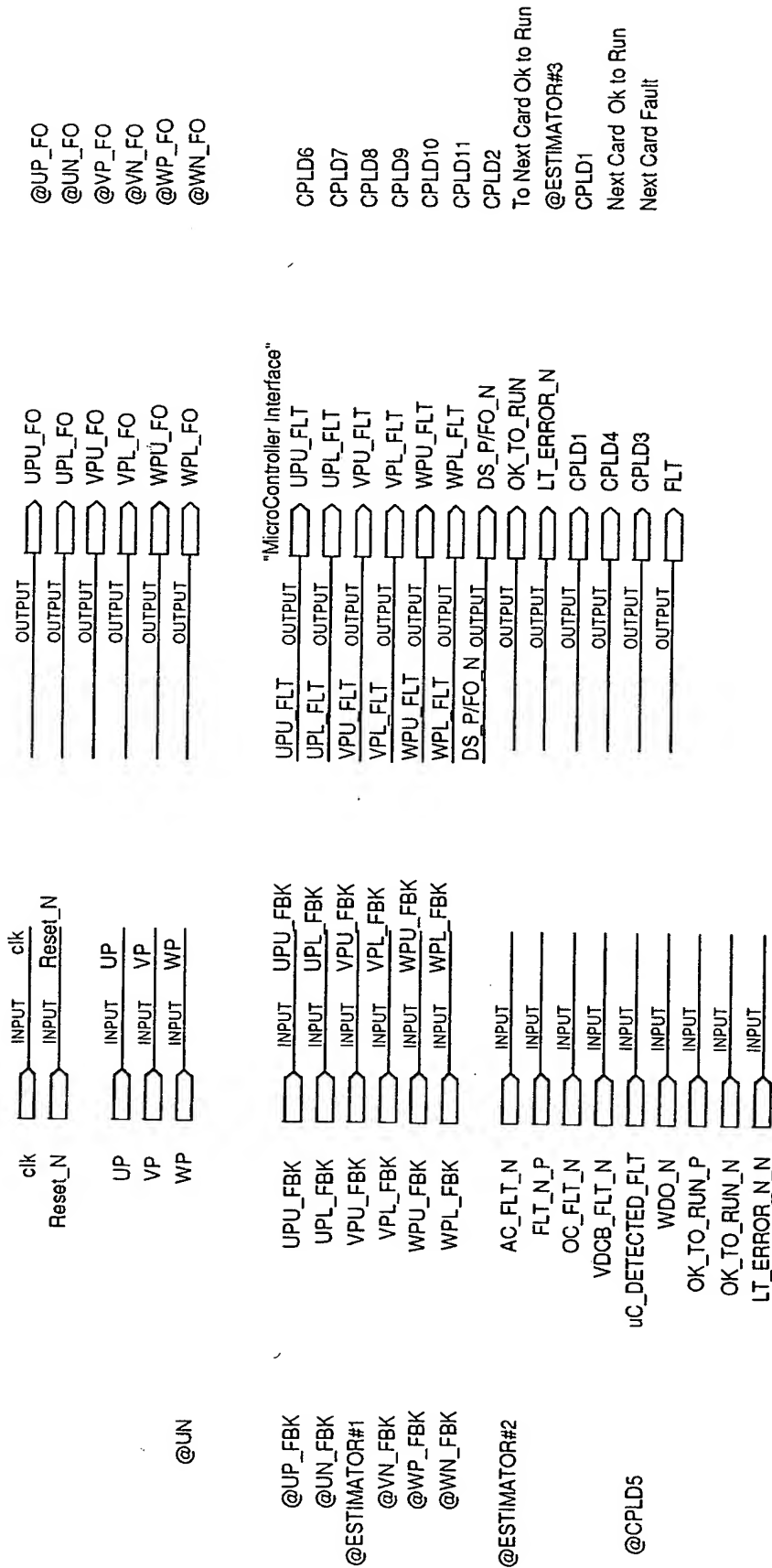


FIG. 17D

FIG. 17E

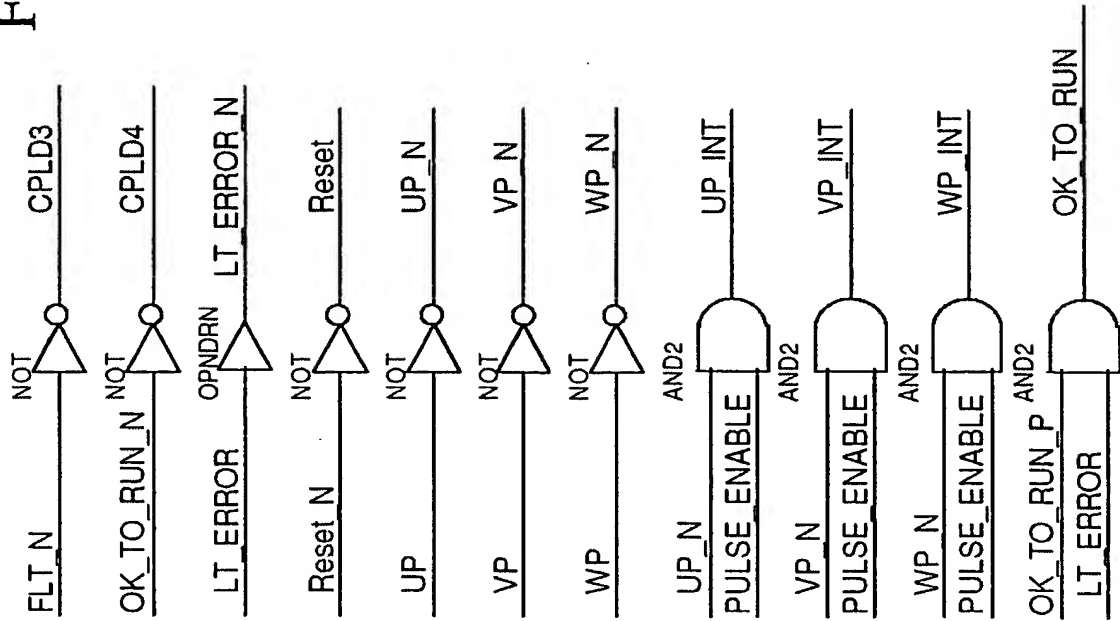
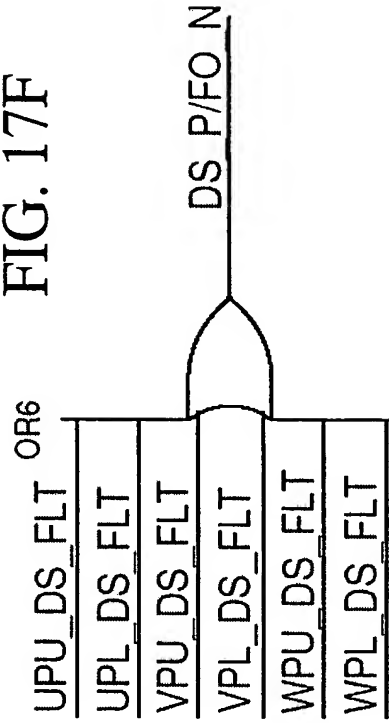


FIG. 17F



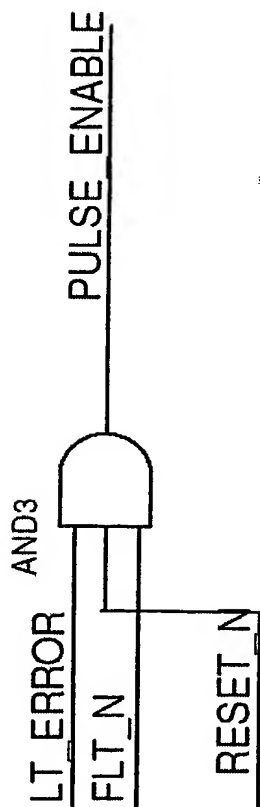


FIG. 17G

FIG. 17H

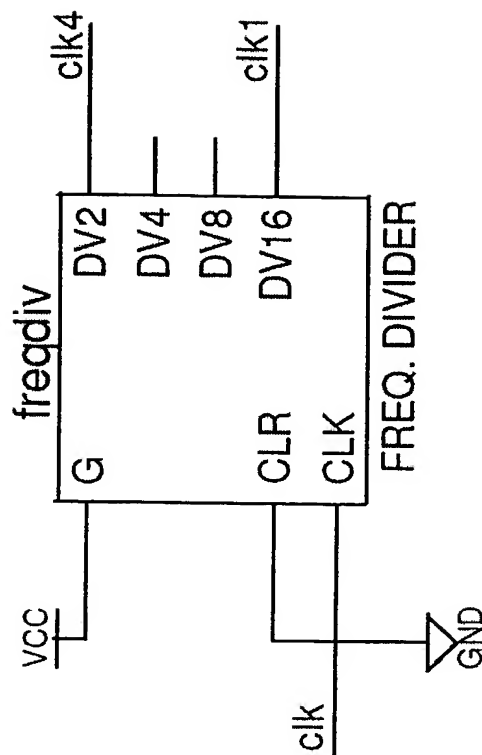


FIG. 17I

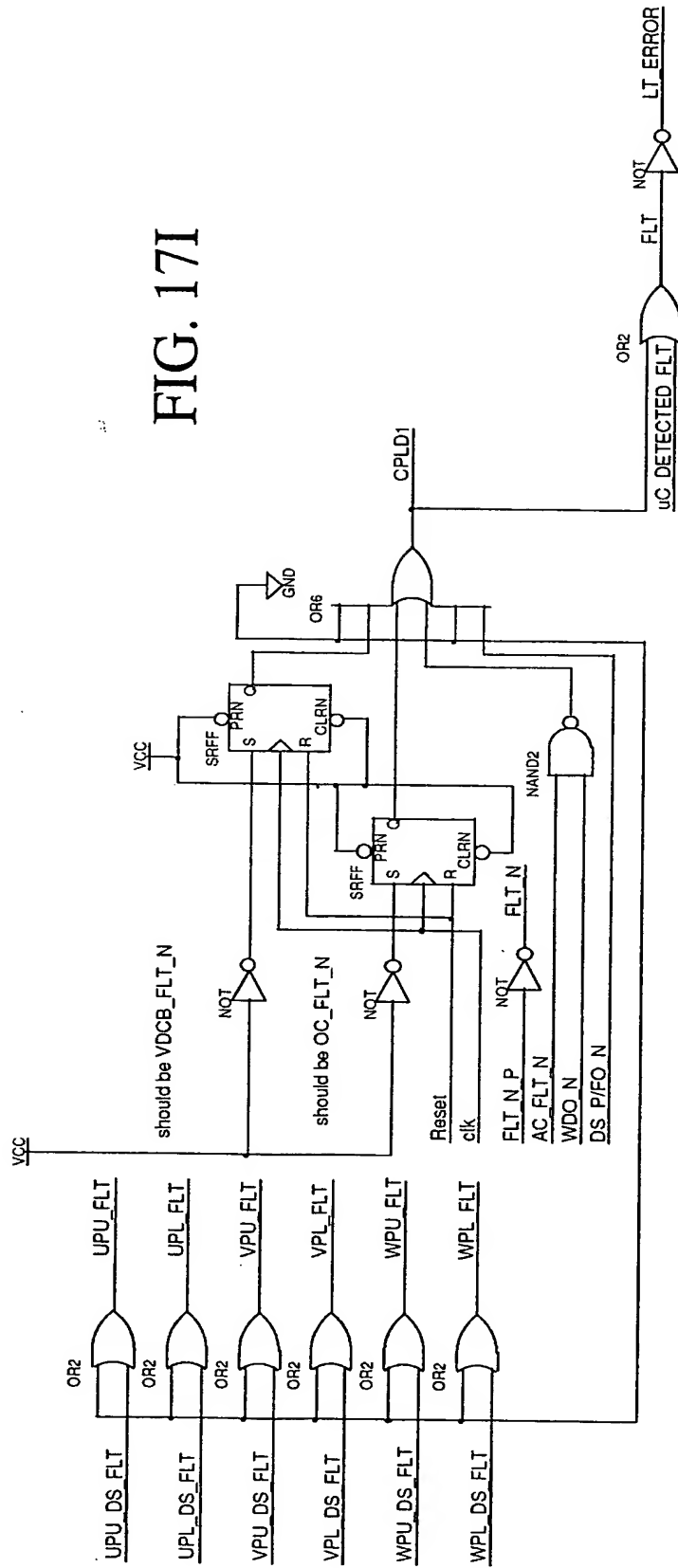


FIG. 17J

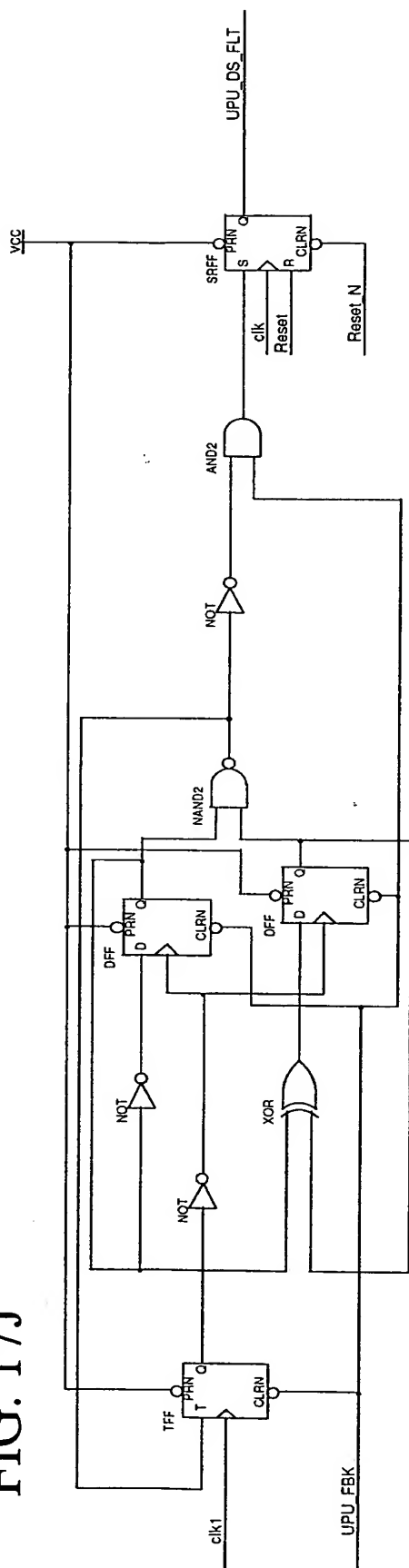


FIG. 17K

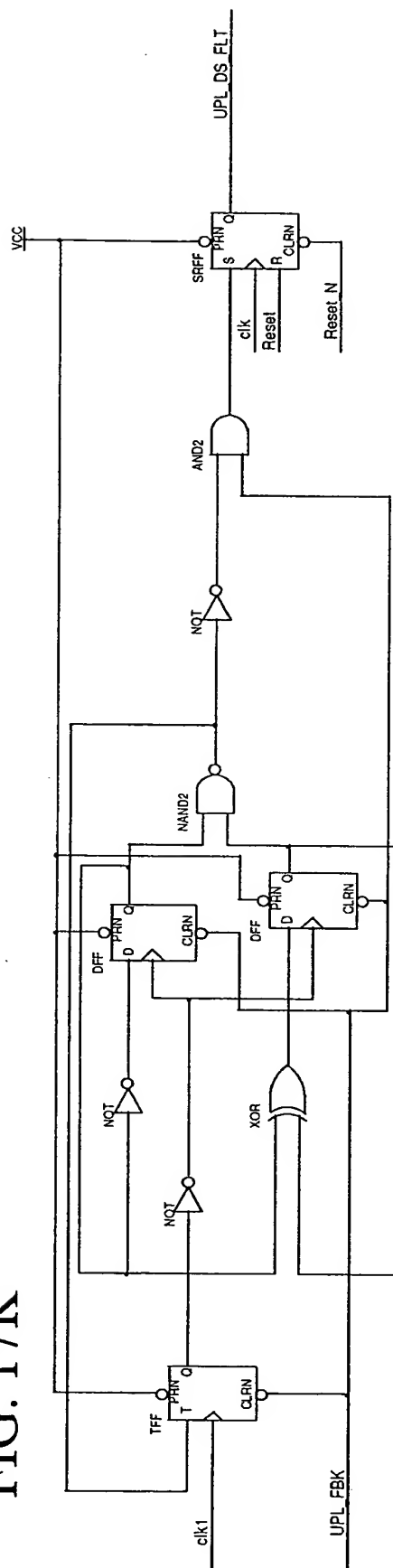


FIG. 17M

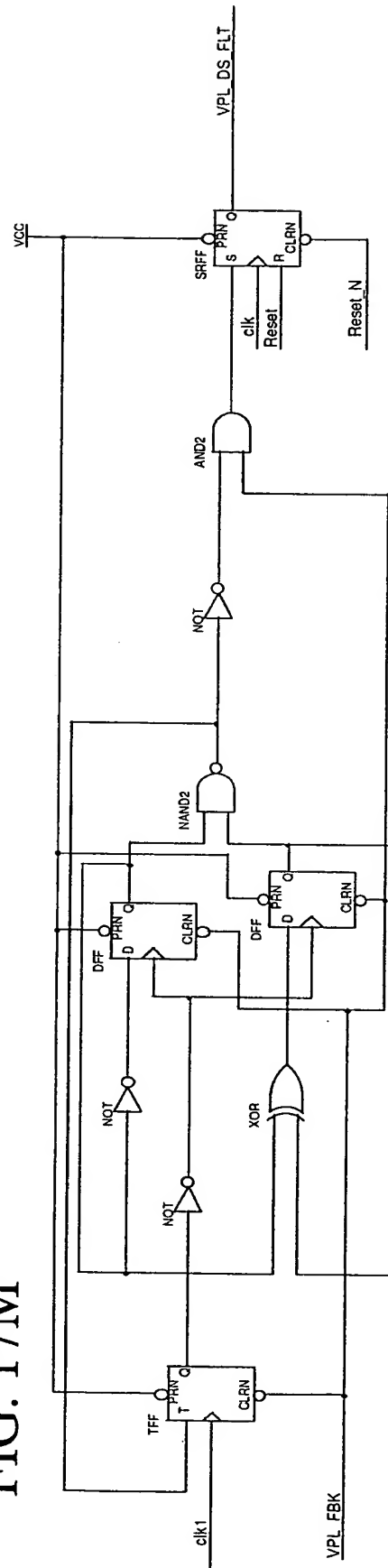


FIG. 1/N

**FIG. 170**

The logic diagram shows a digital circuit with the following components and connections:

- Inputs:** `clk1`, `WPL DS FLT`, `WPL FBK`, and `VCC`.
- Outputs:** `TFF`, `SRRFF`, and `Reset_N`.
- Flip-Flops:**
  - Top D Flip-Flop:** `D` input is `NOT(DFF)`; `PRN` (preset) is `VCC`; `CLR_N` (clear) is `WPL DS FLT`; `Q` output is `TFF`.
  - Bottom D Flip-Flop:** `D` input is `NOT(DFF)`; `PRN` is `VCC`; `CLR_N` is `WPL DS FLT`; `Q` output is `SRRFF`.
- Multiplexers:**
  - Top 2-to-1 MUX:** `D` input is `NOT(DFF)`; `PRN` is `VCC`; `CLR_N` is `WPL DS FLT`; `Q` output is `TFF`.
  - Bottom 2-to-1 MUX:** `D` input is `NOT(DFF)`; `PRN` is `VCC`; `CLR_N` is `WPL DS FLT`; `Q` output is `SRRFF`.
- Logic Gates:**
  - AND2:** Inputs are `clk1` and `WPL DS FLT`; output is `Reset_N`.
  - NAND2:** Inputs are `clk1` and `WPL DS FLT`; output is `Reset_N`.
  - XOR:** Inputs are `clk1` and `WPL DS FLT`; output is `Reset_N`.
  - NOT:** Inverters for `DFF` and `Reset_N`.

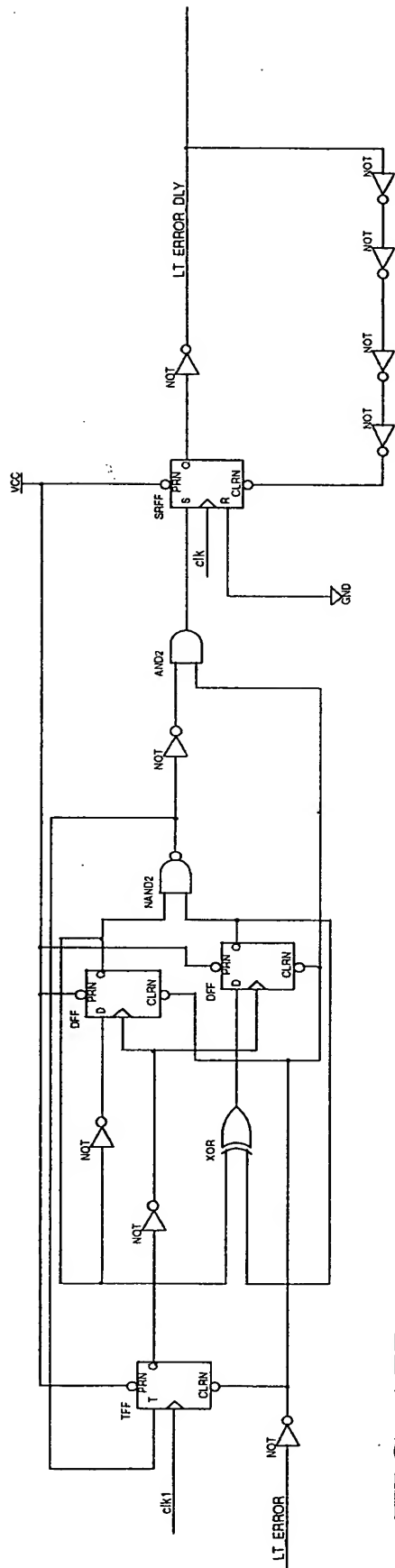


FIG. 17P

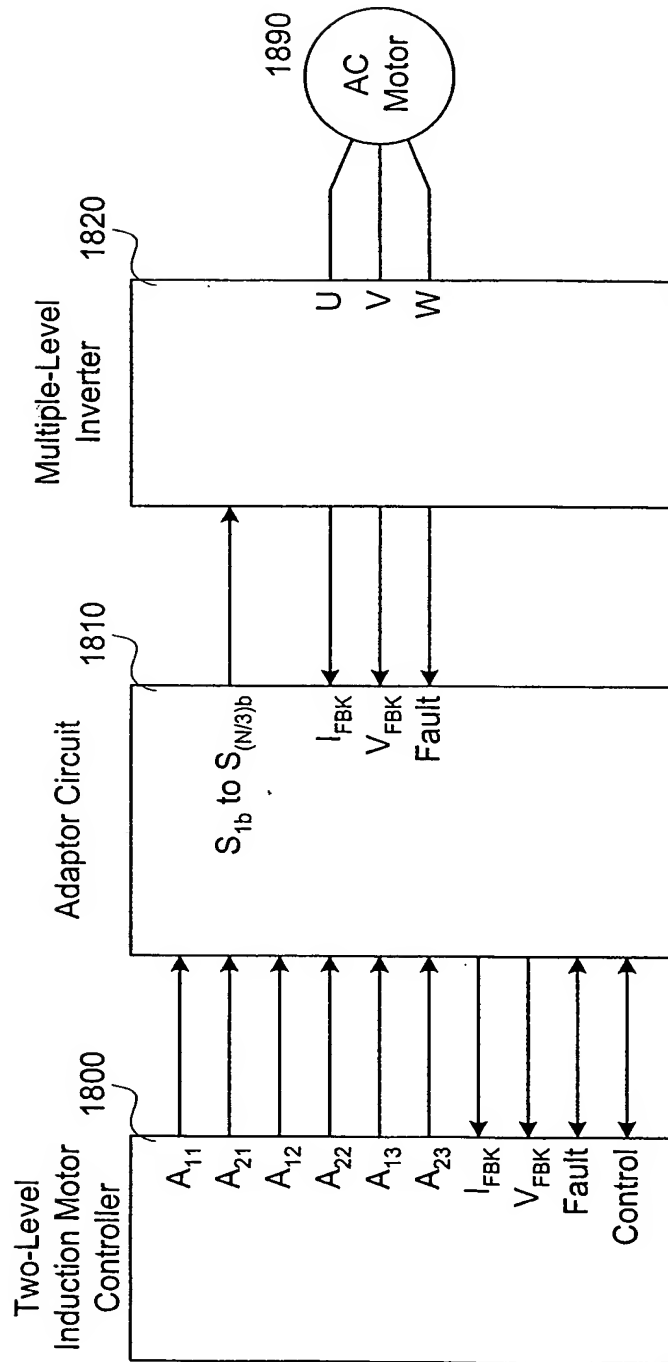


FIG. 18

FIG. 19

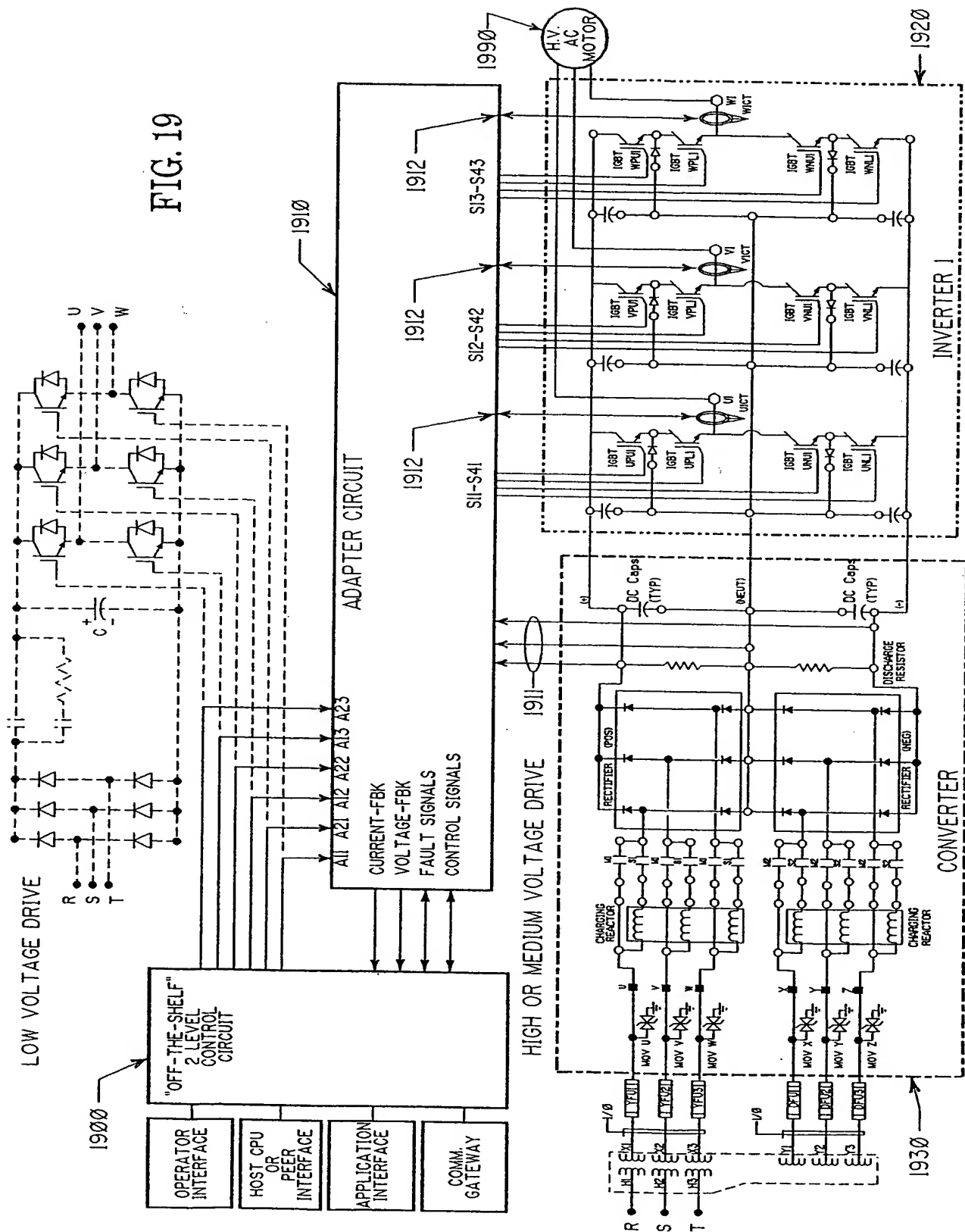


FIG. 20A

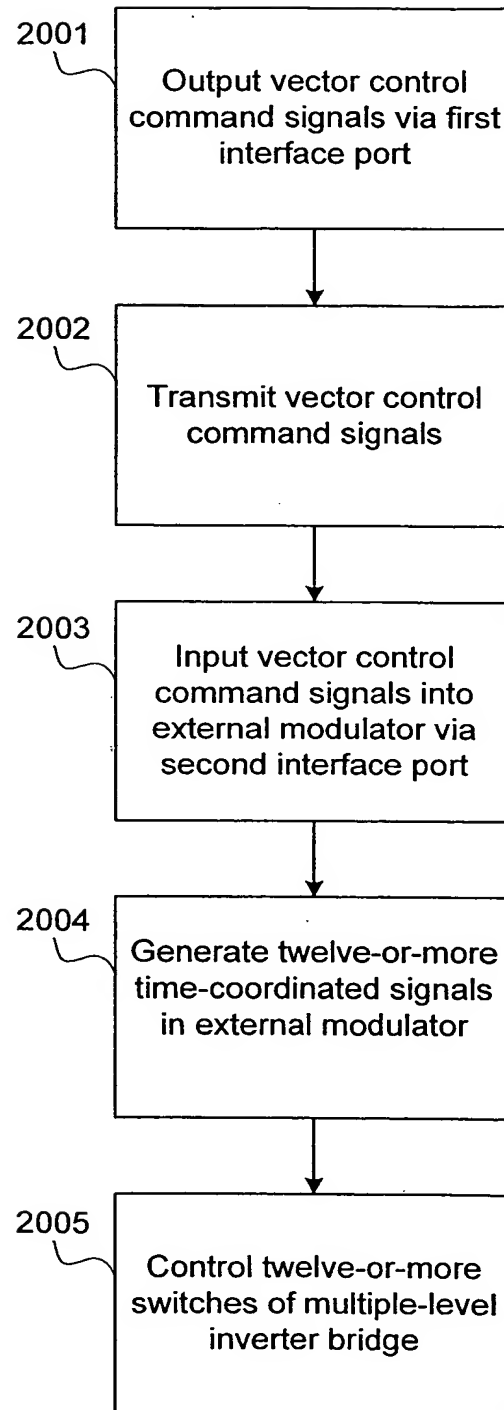
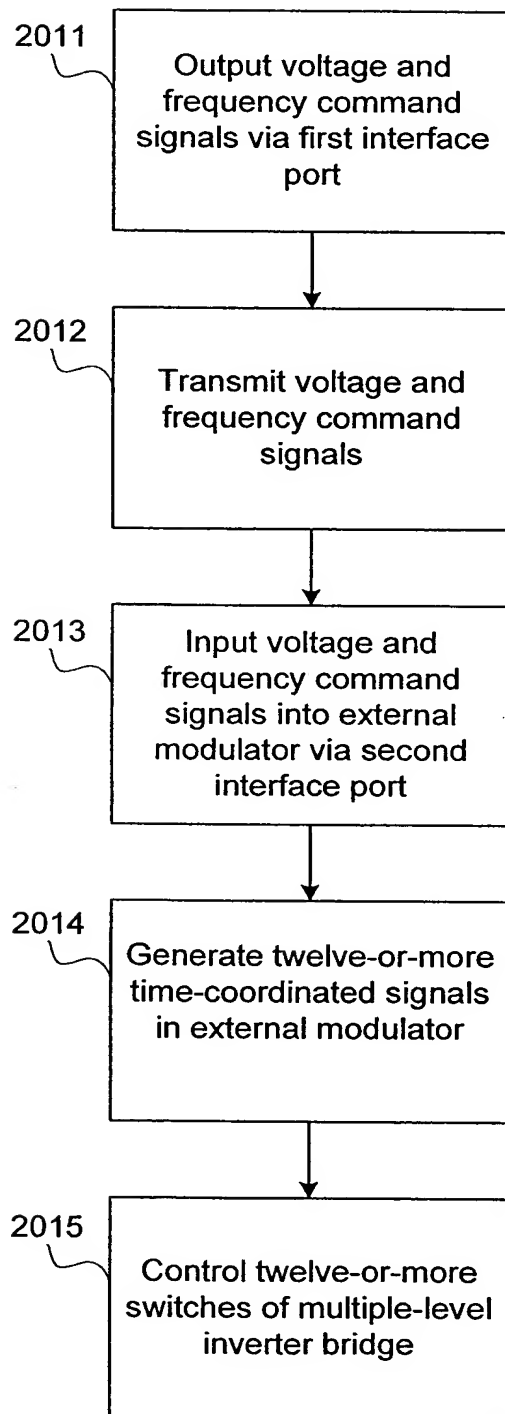


FIG. 20B



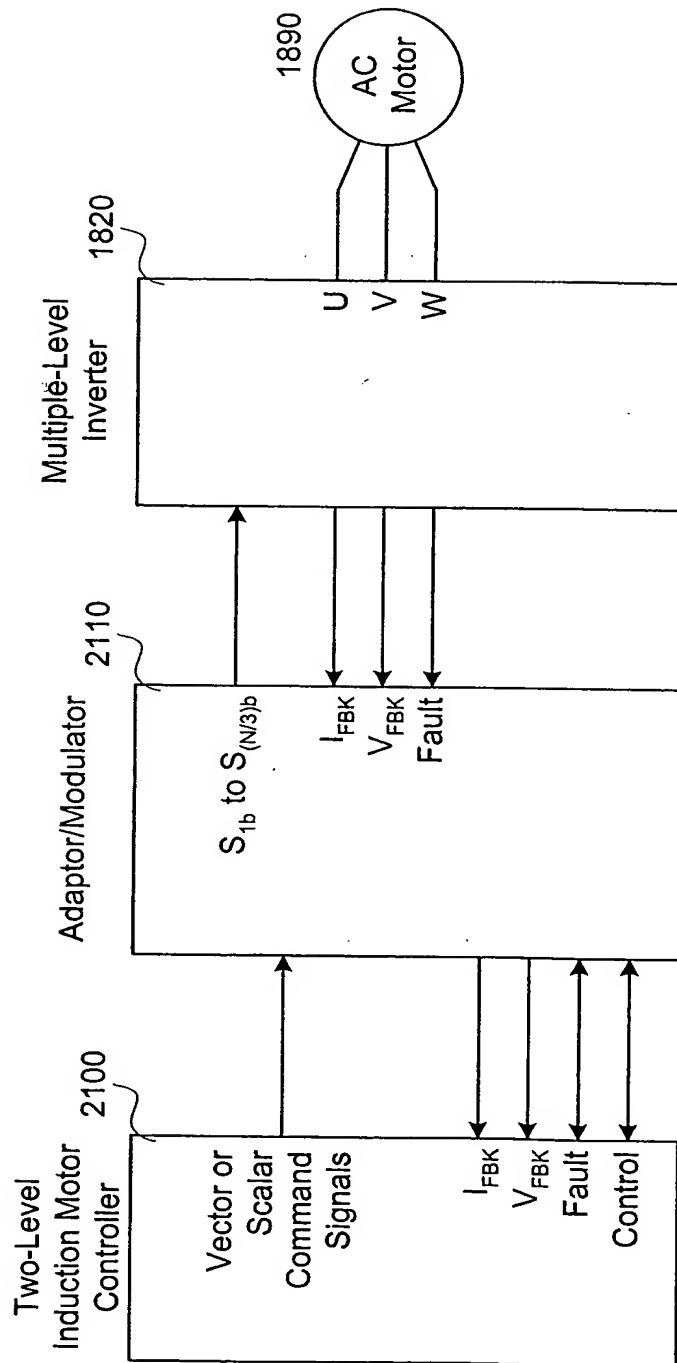
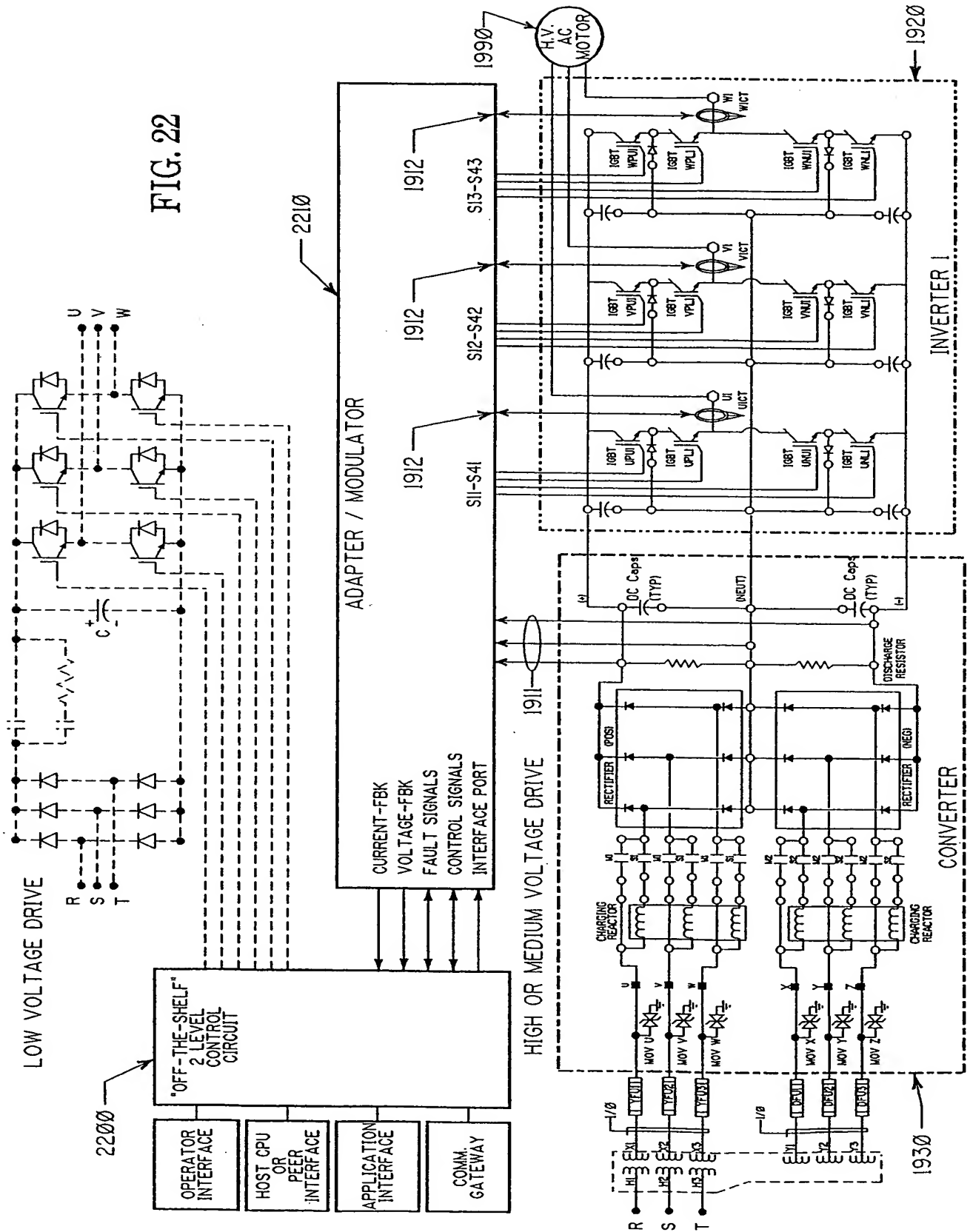


FIG. 21



32/41

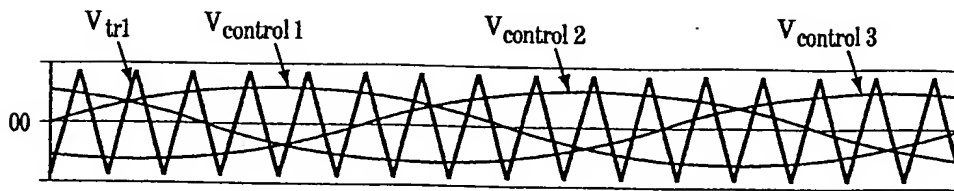


FIG. 23A

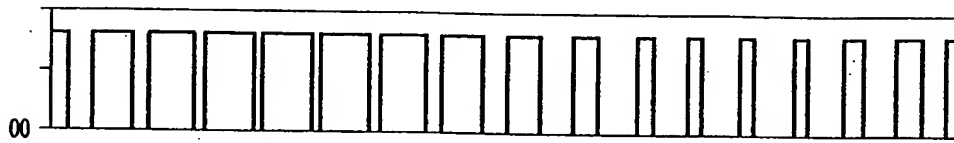


FIG. 23B

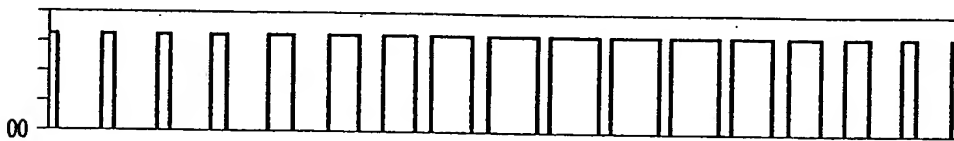


FIG. 23C

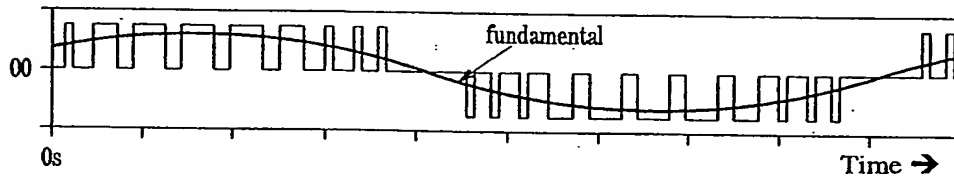


FIG. 24

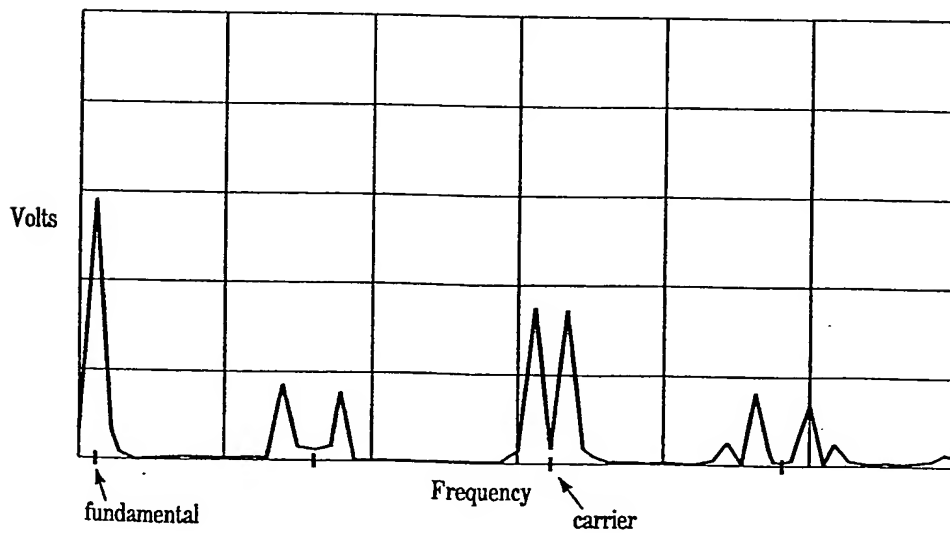


FIG. 25

33/41

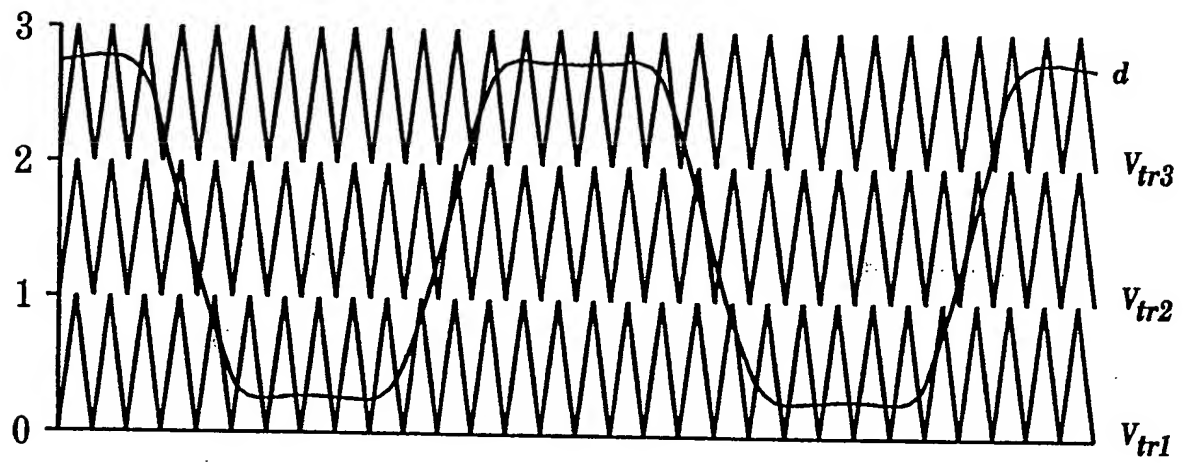


FIG. 26A

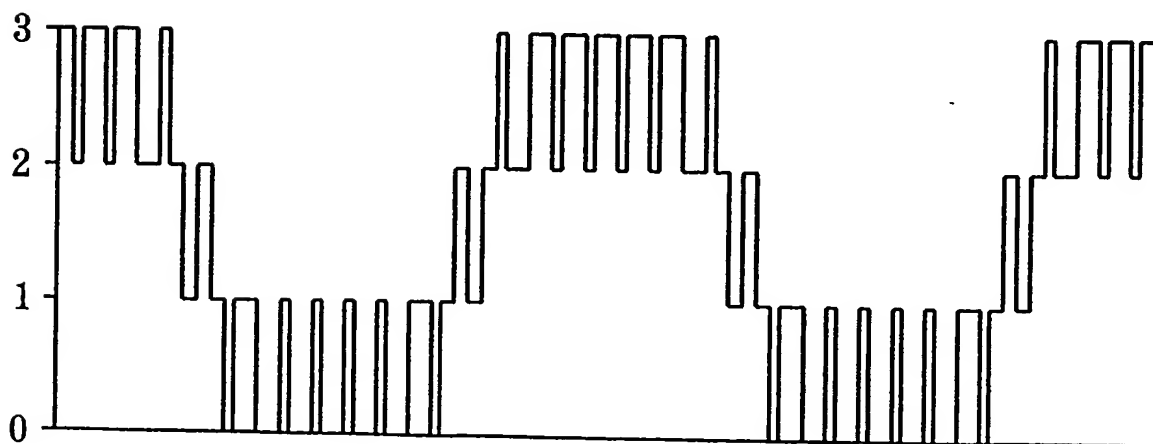
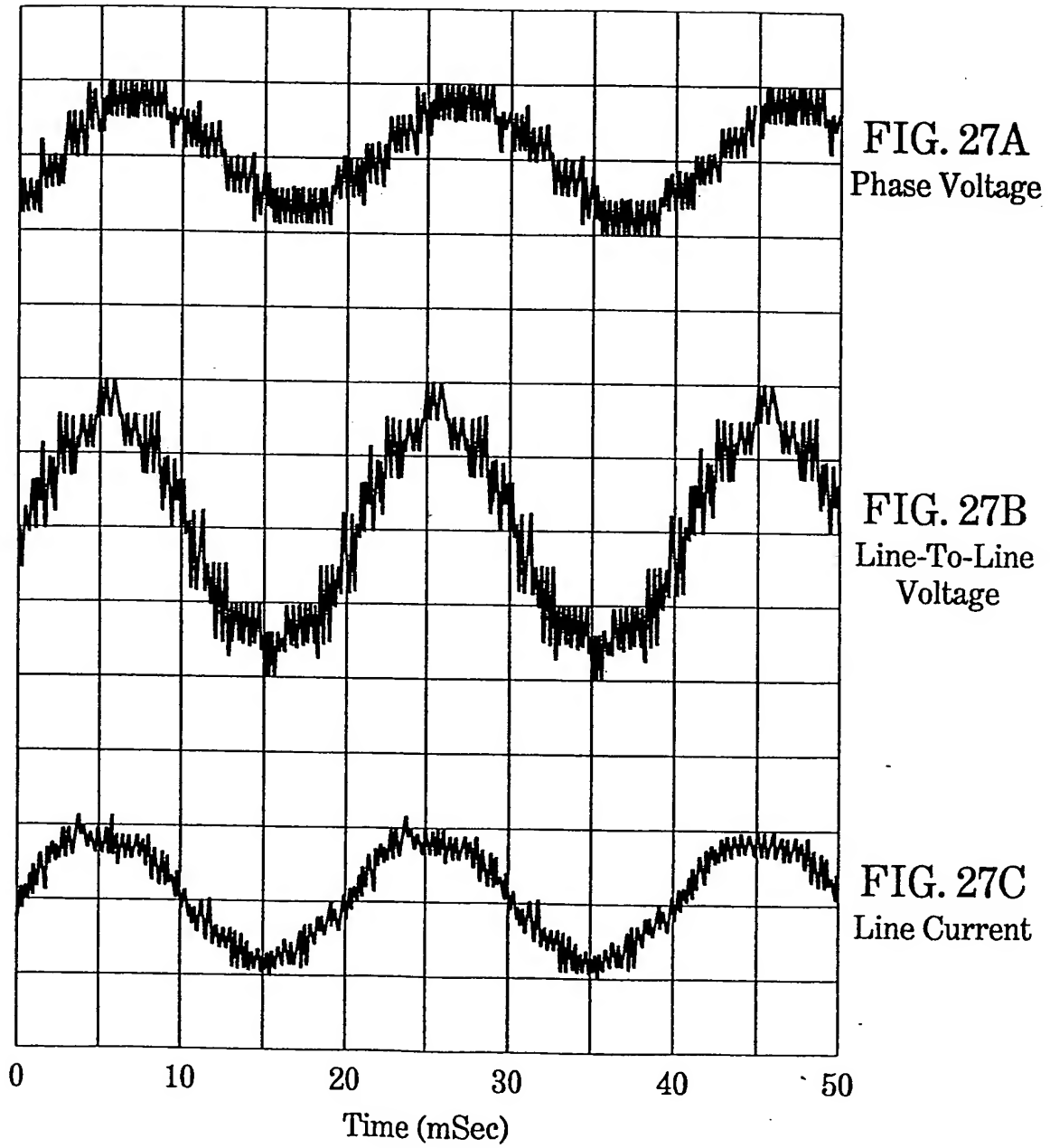


FIG. 26B

34/41



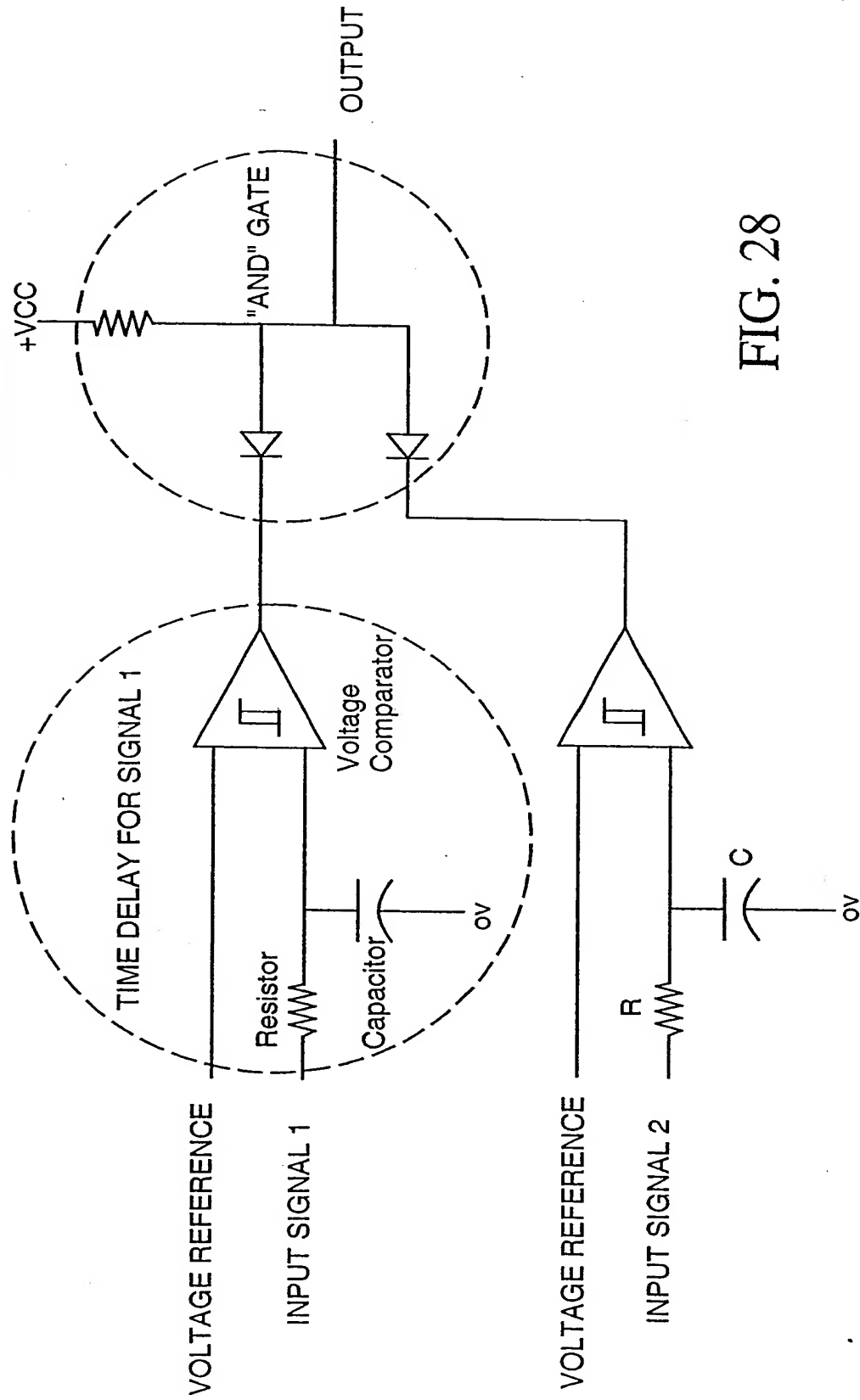
EQUIVALENT PARTIAL LOGIC IMPLEMENTED WITH ANALOG CIRCUIT

FIG. 28

# Off-the-Shelf Induction Motor Controller with Vector Control with Space Vector Modulator

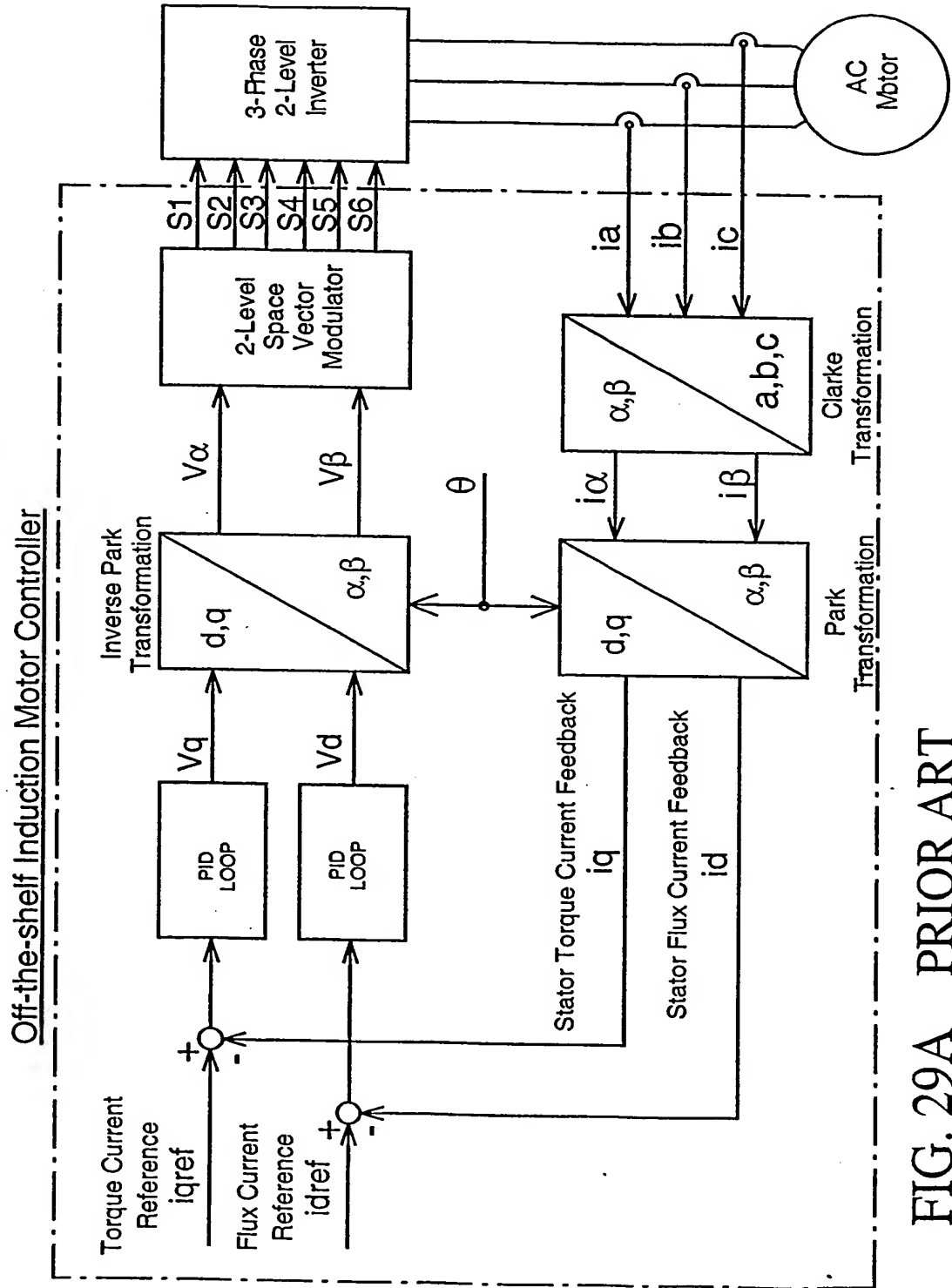


FIG. 29A PRIOR ART

# Off-the-Shelf Induction Motor Controller with Vector Control with Sine-Triangle Modulator

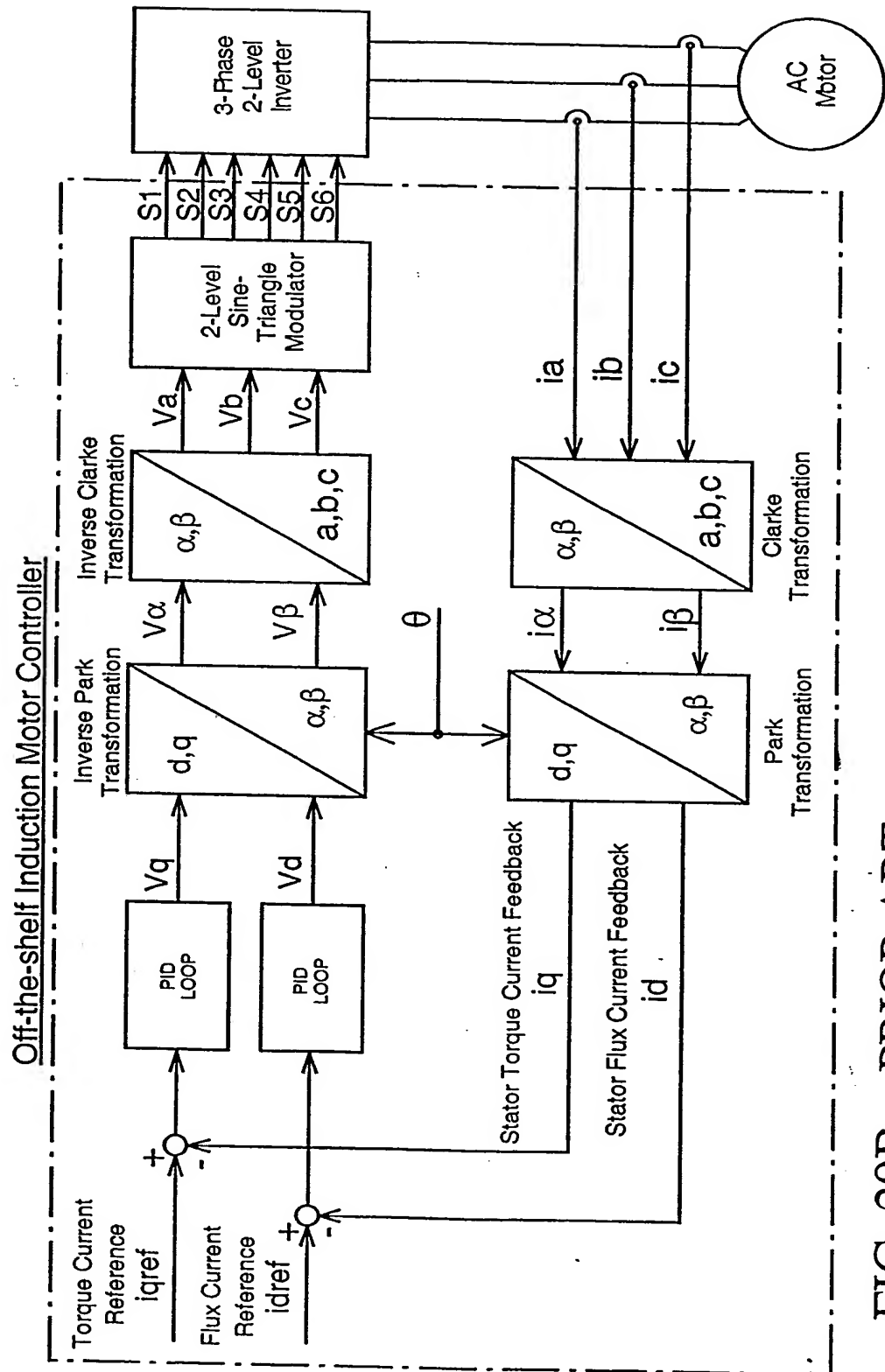


FIG. 29B PRIOR ART

Example of the Second Variation of the Invention with  
Space Vector Modulator

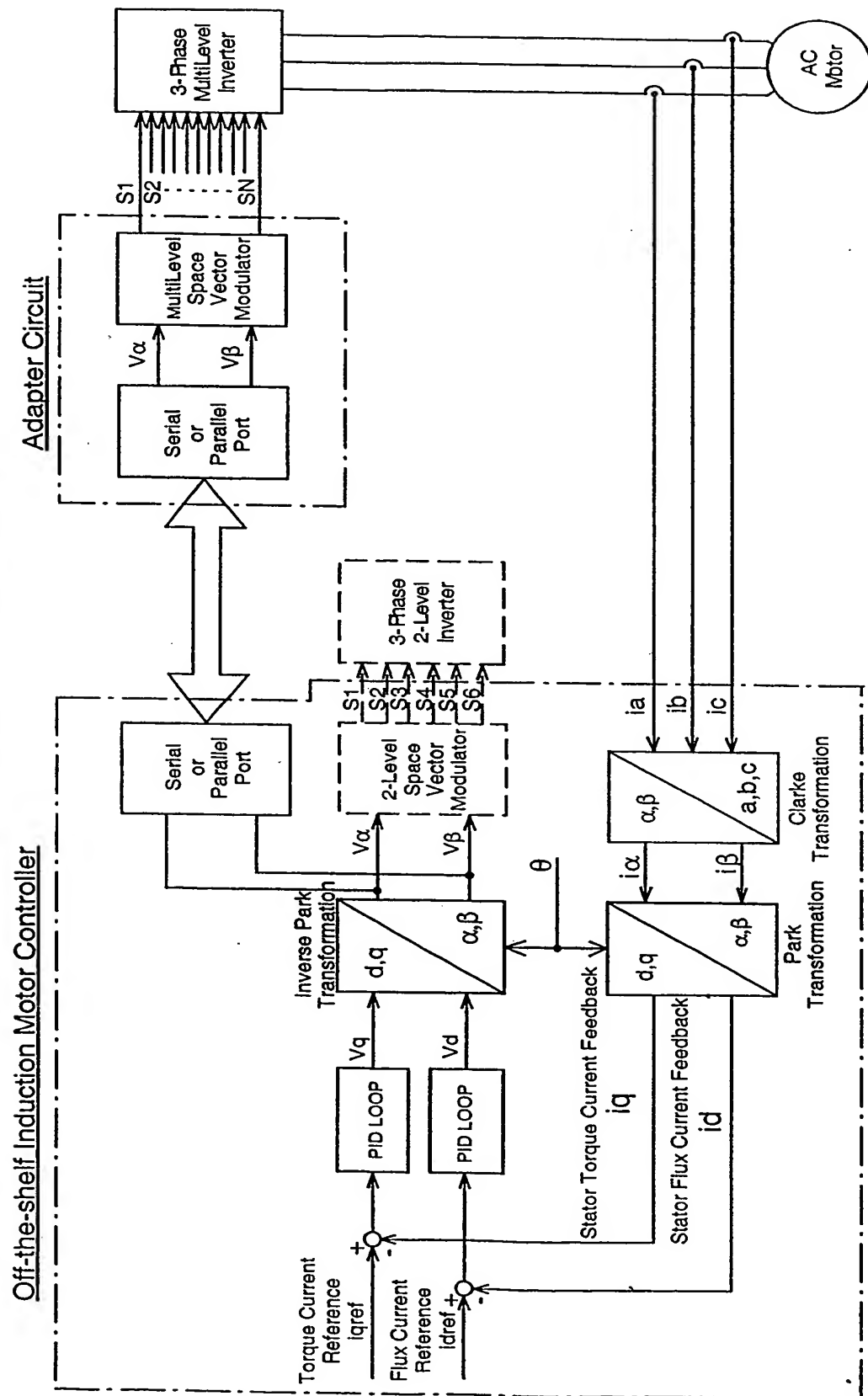


FIG. 30A

Example of the Second Variation of the Invention with Sine-Triangle Modulator

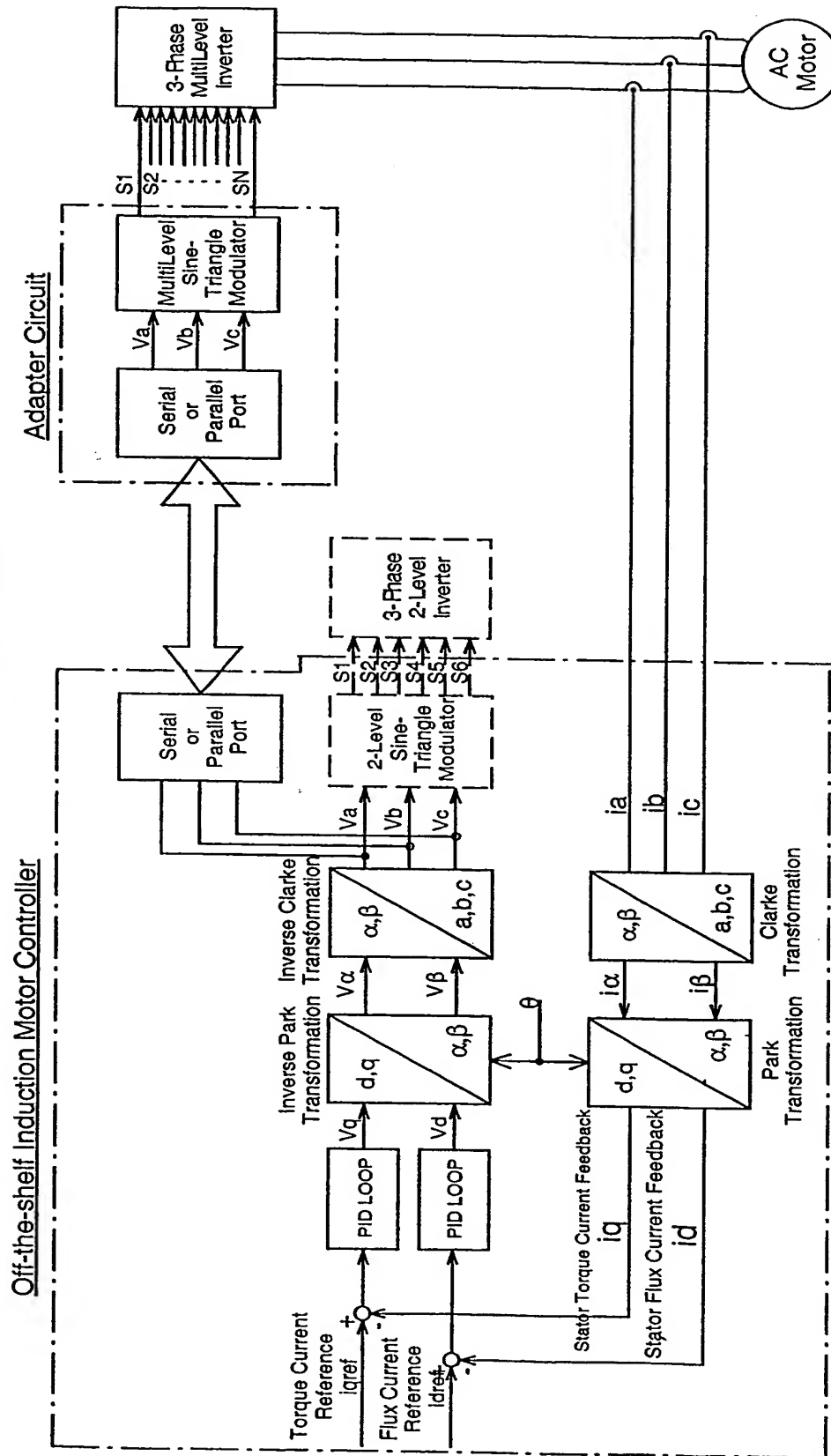


FIG. 30B

Example of the Second Variation of the Invention with Mathematical Transformations and Sine-Triangle Modulator

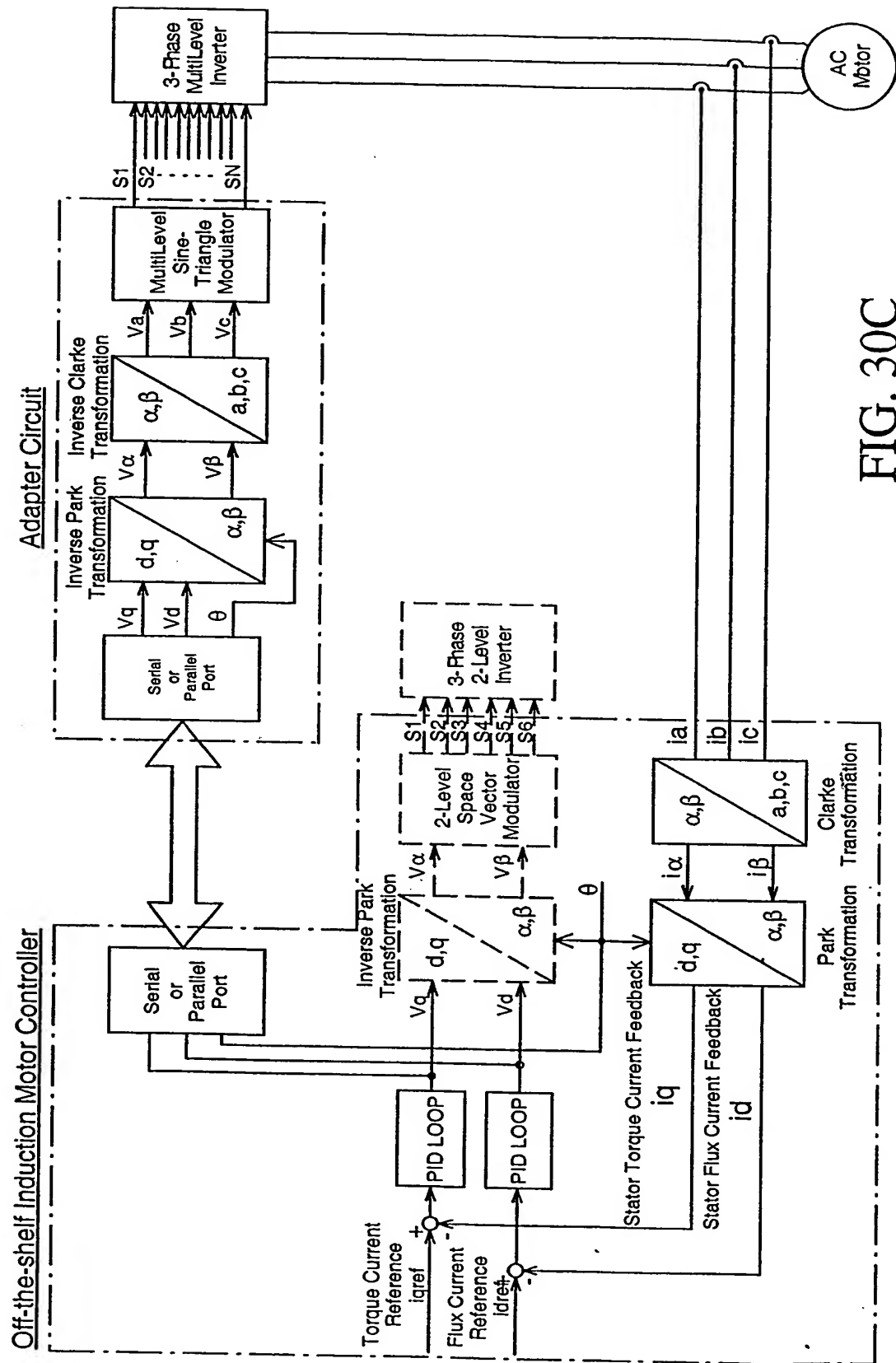


FIG. 30C

Example of the Second Variation of the Invention with Mathematical Transformation and Space Vector Modulator

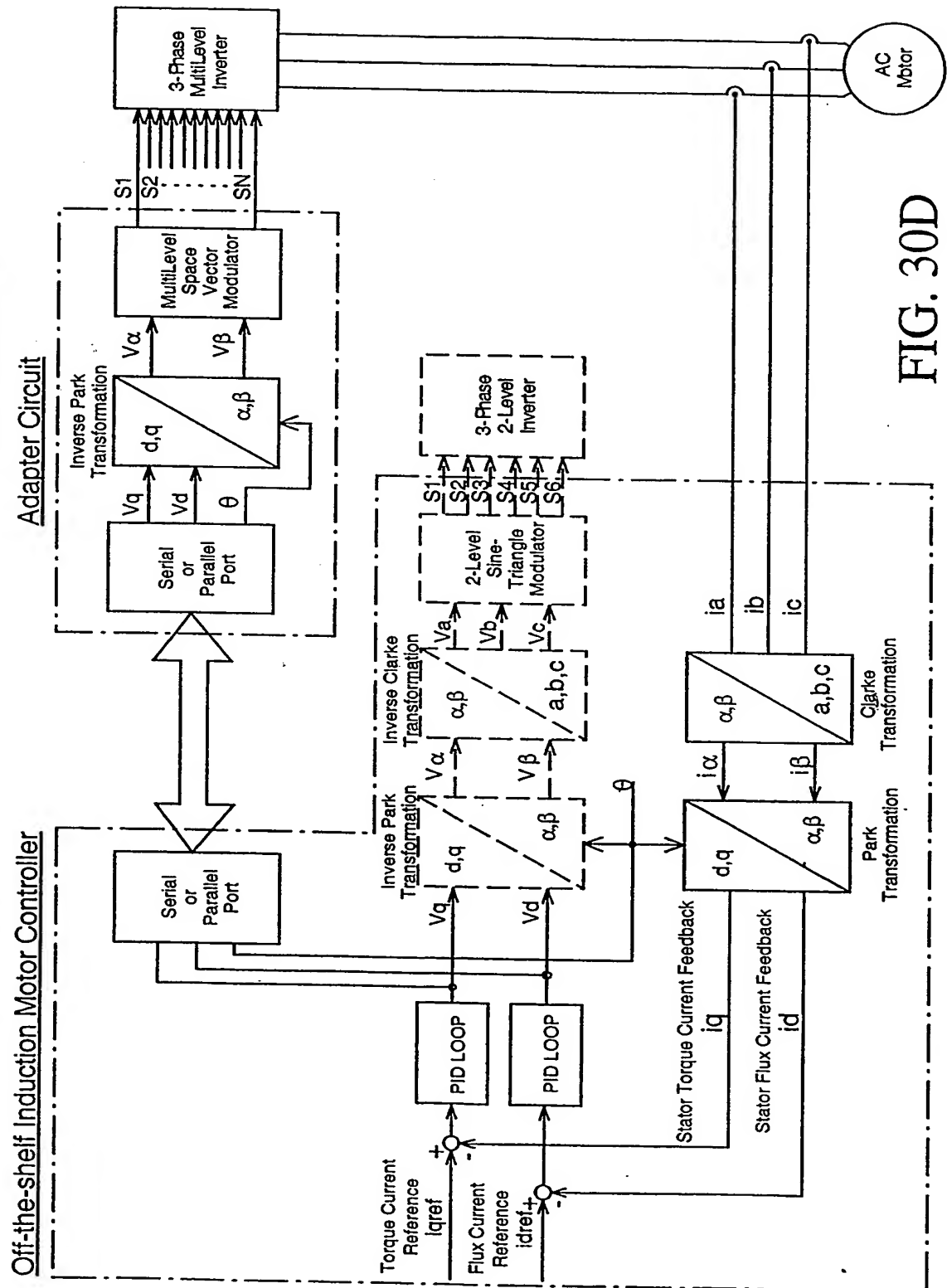


FIG. 30D